FN-LINK欧智通

PRODUCT SPECIFICATION

V200Z-R

AIOT Wi-Fi/Bluetooth Combo Module

Version: v1.3

V200Z-R Module Datasheet

	Part NO.	Description
Ordering Information	FGV200ZRXX-00	BES2600, Wi-Fi dual-band, a/b/g/n 1T1R, BT5.2, on-chip 16MB PSRAM and 16MB Flash, 28X20mm, with shielding, printing antenna
	FGV200ZRXX-01	BES2600, Wi-Fi dual-band, a/b/g/n 1T1R, BT5.2, on-chip 40MB PSRAM and 32MB Flash, 28X20mm, with shielding, printing antenna

Customer: _____

Customer P/N:_____

Signature:_____

Date:_____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

TEL:+86-755-2955-8186 Website:www.fn-link.com

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Revision History

Version	Date	Contents of Revision Change	Draft	Checked	Approved
V1.0	2021/10/25	New version	FC	LSP	QJP
V1.1	2021/12/29	Refine RF spec, add EVB info, add package info, update marking info and ordering info.	FC	LSP	QJP
V1.2	2022/04/27	Refine RF spec Modify Pin Definition	FC	LSP	QJP
V1.3	2022/05/13	Update packaging information	FC	LSP	QJP

1. General Description

1.1 Introduction

V200Z-R is a highly integrated wireless module with voice & audio functions. It is based on BES2600 solution which features a Cortex-M33 Star dual-core MCU subsystem and a Cortex-A7 dual-core AP subsystem. Both MCU and AP subsystem are able to run RTOS and user applications.

The module supports low power Wi-Fi 4 (1x1 802.11a/b/g/n dual-band) and Bluetooth 5.2 dual-mode (support BT/BLE, LE Audio). Besides, it provides a high-performance on-board printing antenna to reduce the complexity of hardware design.

V200Z-R also provides a voice & audio CODEC subsystem and a display subsystem with 2D graphics engine. It supports MIPI DSI HD display up to HD (720P60), supports MIPI CSI Camera up to 2MPixel, and supports microphone arrays with up to three analog microphones or six digital microphones for far-field voice application. MCU subsystem runs Bluetooth upper protocol stack, and AP subsystem and 2D hardware Graphics Engine can accelerate GUI & VUI, voice & audio processing and AI tasks.

This compact module is a perfect choice for smart appliance, smart panel, entrance guard and other smart home applications.

1.2 Description

Model Name	V200Z-R
Product Description	Support Wi-Fi & Bluetooth, voice & audio, LCD & camera
Dimension	L x W x H: 28 x 20 x2.55 mm
Interface	USB2.0, UART, I2C, I2S, SDIO device, MIPI, PWM, GPIO
OS	RTOS, OpenHarmony
Operating temperature	-20°C to 80°C
Storage temperature	-30°C to 125°C

1.3 EVB information

Fn-Link provides a evaluation suite for the development and test of V200Z-R module. It includes an evaluation board, a 4 inch LCD module, a camera Module and USB type-C cable.

Please contact Fn-Link sales for EVB documentation and ordering.

2. Features

CPU

- CMOS single-chip fully-integrated PMU, CODEC, RF, BB, MCU and AP subsystem
- 300MHz ARM Cortex-M33 Star dual-core MCU subsystem
- 1GHz ARM Cortex-A7 dual-core AP subsystem with NEON.
- Shared 2MB SRAM, on-chip PSRAM and on-chip NOR flash[Note1]
- Support TrustZone and secure boot

Wi-Fi / BT

- 2.4GHz & 5GHz dual-band Wi-Fi, 1T1R, compliant to IEEE 802.11a/b/g/n
- Support 20MHz and 40MHz bandwidth
- Bluetooth 5.2 dual-mode
- Support BLE Mesh and LE audio
- A2DP v1.3/AVRCP v1.5/HFP v1.6
- Wi-Fi and Bluetooth co-existence

Audio

- Hi-Fi Stereo Audio DAC and ADC
- Far-field voice wake up
- 24bit audio processing
- Support Acoustic Echo Cancellation
- Support DSD-64/128/256 decode

Peripheral interfaces

- MIPI Tx DSI and MIPI Rx CSI interface
- USB2.0 HS Host or Device
- 4x UART interface, with flow control and configurable baud rate
- 50Mbps SPIx2, with serial LCD support
- 1.4Mbps I2C master x3
- I2S/TDM
- PWMx8
- 10-bit GPADC, 3 channels

Note1: Please refer to ordering information for detailed memory size.

3. General Specification

3.1 Wi-Fi 2.4GHz Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400GHz ~ 2.4835GHz (2.4GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 17 ± 2 dBm	EVM ≤ -10dB
	802.11g /54Mbps : 16 ± 2 dBm	EVM ≤ -25dB
	802.11n /MCS7 : 15 ± 2 dBm	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
SISO Receive Sensitivity (11b) @8% PER	- 1Mbps PER @ -95 dBm	
	- 11Mbps PER @ -86 dBm	
SISO Receive Sensitivity (11g) @10% PER	- 6Mbps PER @ -88 dBm	
	- 54Mbps PER @ -73 dBm	
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -88 dBm	
	- MCS=7 PER @ -70 dBm	
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 PER @ -85 dBm	
	- MCS=7 PER @ -66 dBm	
Maximum Input Level	802.11b : -8 dBm	
	802.11g/n : -20 dBm	

3.2 Wi-Fi 5GHz Specification

Feature	Description	
WLAN Standard	IEEE 802.11 a/n Wi-Fi compliant	
Frequency Range	5.18GHz ~ 5.825GHz	
Number of Channels	Please refer to table[1]	
Test Items	**Typical Value**	**EVM**
	802.11a /54Mbps : 15 ± 2 dBm	EVM ≤ -25dB
	802.11n /MCS7 : 14 ± 2 dBm	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
SISO Receive Sensitivity	- 6Mbps PER @ -87 dBm	

(11a) @10% PER	- 54Mbps	PER @ -70 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0	PER @ -86 dBm
	- MCS=7	PER @ -68 dBm
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0	PER @ -83 dBm
	- MCS=7	PER @ -65 dBm
Maximum Input Level	802.11a : -20 dBm	
	802.11n : -20 dBm	

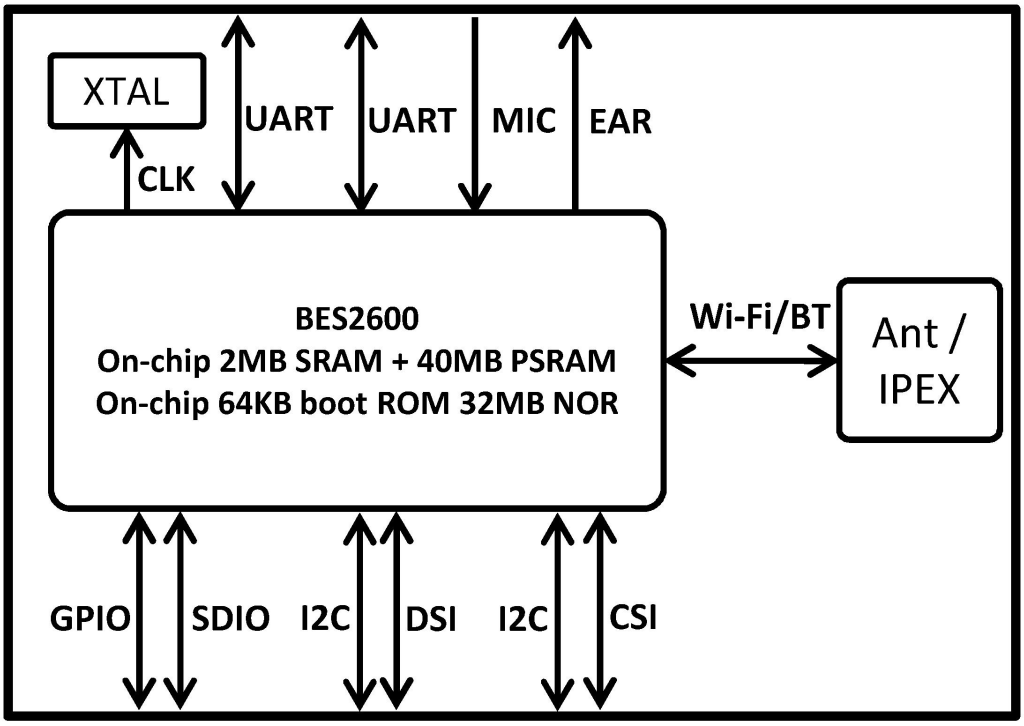
[1]5GHz(20MHz) Channel table

Band range	Operating Channel	Channel center frequency (MHz)
5180MHz~5240MHz	36	5180
	40	5200
	44	5220
	48	5240
5260MHz~5320MHz	52	5260
	56	5280
	60	5300
	64	5320
5550MHz~5700MHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640
	132	5660
	136	5680
	140	5700
5745MHz~5825MHz	149	5745
	153	5765
	157	5785
	161	5805
	165	5825

3.3 Bluetooth Specification

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V5.2		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels for BDR/EDR, 40 channels for BLE		
Modulation	GFSK, π/4-DQPSK, 8-DPSK		
RF Specification			
	Min.	**Typical.**	**Max.**
Output Power - BDR/LE		8dBm	
Output Power - EDR		6dBm	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-91dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-89dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-83dBm	
Sensitivity @ PER < 30.8% for BLE		-90dBm	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

4. Block Diagram



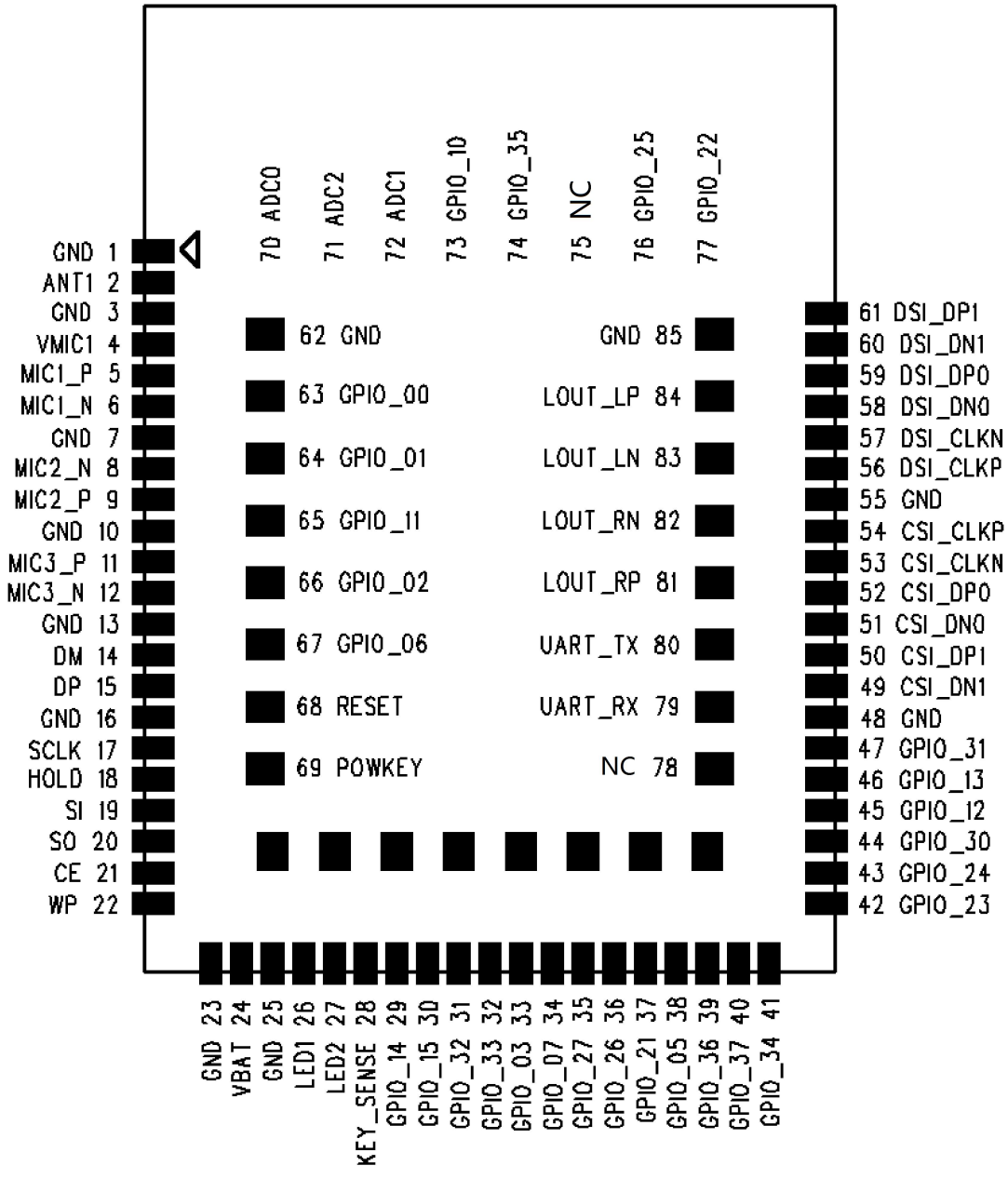
*5. ID setting information

TBD.

6. Pin Definition

6.1 Pin Outline

< TOP VIEW >



6.2 Pin Definition details

NO	Name	Type	Description	Voltage
1	GND	-	Ground connections	
2	ANT1[Note2]	Analog	Optional Wi-Fi&BT Antenna port, for external antenna	
3	GND	-	Ground connections	
4	VMIC1	Analog	Bias voltage output for external MIC devices. Output range 1.5~3.3V. Suggest 1uF decoupling capacitor and RC filter.	
5	MIC1_P	Analog	MIC1 P port, maximum input voltage 1.8V (P to GND), pin requires blocking capacitor.	
6	MIC1_N	Analog	MIC1 N port, maximum input voltage 1.8V (P to GND), pin requires blocking capacitor.	
7	GND	-	Ground connections	
8	MIC2_N	Analog	MIC2 N port, please refer to the description of MIC1	
9	MIC2_P	Analog	MIC2 P port, please refer to the description of MIC1	
10	GND	-	Ground connections	
11	MIC3_P	Analog	MIC3 P port, please refer to the description of MIC1	
12	MIC3_N	Analog	MIC3 N port, please refer to the description of MIC1	
13	GND	-	Ground connections	
14	DM	Analog	USB2.0 D-, support high speed and full speed	
15	DP	Analog	USB2.0 D+, support high speed and full speed	
16	GND	-	Ground connections	
17	SCLK	I/O	External Flash serial clock	1.8V
18	HOLD	I/O	External Flash Hold	1.8V
19	SI	I/O	External Flash serial input	1.8V
20	SO	I/O	External Flash serial output	1.8V
21	CE	I/O	External Flash Chip Enable	1.8V
22	WP	I/O	External Flash Write Protect	1.8V
23	GND	-	Ground connections	
24	VBAT	Analog	VBAT power supply input, range 3.1~5.5V, typically 3.8V. This pin requires external filter capacitor.	
25	GND	-	Ground connections	
26	LED1	O	LED pin, PMU peripheral IO. Suggest cathode drive mode. Maximum sink current 5mA. Internally PU by default,	
27	LED2	O	LED pin, please refer to the description of LED1.	
28	KEY_SENSE	I/O	Keypad sense pin, 10-bit ADC input with interrupt function. Max. measurable voltage 1.7V. Max. input voltage 2.5V.	
29	GPIO_14	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO[Note3]

30	GPIO_15	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
31	GPIO_32	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
32	GPIO_33	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
33	GPIO_03	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
34	GPIO_07	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
35	GPIO_27	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
36	GPIO_26	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
37	GPIO_21	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
38	GPIO_05	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
39	GPIO_36	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
40	GPIO_37	I/O	GPIO, please refer to GPIO MUX Mapping for details, low-level cathode drive is not recommended,	VDDIO
41	GPIO_34	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
42	GPIO_23	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
43	GPIO_24	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
44	GPIO_30	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
45	GPIO_12	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
46	GPIO_13	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
47	GPIO_31	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
48	GND	-	Ground connections	
49	CSI_DN1	I/O	CMOS sensor interface , Channel1_DATA_Negative	
50	CSI_DP1	I/O	CMOS sensor interface , Channel1_DATA_Positive	
51	CSI_DN0	I/O	CMOS sensor interface , Channel0_DATA_Negative	
52	CSI_DP0	I/O	CMOS sensor interface , Channel0_DATA_Positive	
53	CSI_CLKN	I/O	CMOS sensor interface , Channel_Clock_Negative	
54	CSI_CLKP	I/O	CMOS sensor interface , Channel_Clock_Positive	
55	GND	-	Ground connections	
56	DSI_CLKP	I/O	Display sensor interface , Channel_Clock_Positive	
57	DSI_CLKN	I/O	Display sensor interface , Channel_Clock_Negative	
58	DSI_DN0	I/O	Display sensor interface , Channel0_DATA_Negative	
59	DSI_DP0	I/O	Display sensor interface , Channel0_DATA_Positive	
60	DSI_DN1	I/O	Display sensor interface , Channel1_DATA_Negative	
61	DSI_DP1	I/O	Display sensor interface , Channel1_DATA_Positive	
62	GND	-	Ground connections	
63	GPIO_00	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
64	GPIO_01	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
65	GPIO_11	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO

66	GPIO_02	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
67	GPIO_06	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
68	RESET	I	Hardware reset input, active high. Keep it > 2/3*VBAT for more than 250ms to achieve a reset.	VBAT
69	POWKEY	I	Hardware power on input, active high. Keep it > 2/3*VBAT for more than 1ms (software configurable).	VBAT
70	ADC0	Analog	ADC channel 0 input, 10-bit, does not support interrupt function. Max. measurable voltage 1.7V. Max. input voltage 2.5V.	
71	ADC2	Analog	ADC channel 2 input, 10-bit, does not support interrupt function. Max. measurable voltage 1.7V. Max. input voltage 2.5V.	
72	ADC1	Analog	ADC channel 1 input, 10-bit, does not support interrupt function. Max. measurable voltage 1.7V. Max. input voltage 2.5V.	
73	GPIO_10	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
74	GPIO_35	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
75	NC		**Please keep it floating**	
76	GPIO_25	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
77	GPIO_22	I/O	GPIO, please refer to GPIO MUX Mapping for details	VDDIO
78	NC		**Please keep it floating**	
79	UART_RX	I	UART0 input, for FW download and debug	VDDIO
80	UART_TX	O	UART0 output, for FW download and debug	VDDIO
81	LOUT_RP	Analog	Channel right differential drive output p port. It is recommended to reserve filter circuit and ESD protector.	
82	LOUT_RN	Analog	Channel right differential drive output n port. It is recommended to reserve filter circuit and ESD protector.	
83	LOUT_LN	Analog	Channel left differential drive output n port. It is recommended to reserve filter circuit and ESD protector.	
84	LOUT_LP	Analog	Channel left differential drive output p port. It is recommended to reserve filter circuit and ESD protector.	
85	GND	-	Ground connections	

Note2: Use on-board antenna by default. Please contact Fn-Link if you prefer external antenna.

Note3: VDDIO = 3.3V by default.

6.3 GPIO MUX Mapping

Maximum source current 10mA for each IO and 50mA for total.

Output state can be configured as strong PU or PL, input state can be configured as high-Z, PU, PL or no pull.

All of them have interrupt function.

GPIO state will be low impedance input when the module is power off, so we do not suggest low level cathode drive mode.

For detailed MUX mapping, please refer to below table.

IO	IO Status	Reference Voltage	Default_Status	IO	Function 0	Function 1	Function 2	Function 3	Function 4	Function 5	Function 6	Function 7	Function 8	Function 9	Function 10	Function 11	Function 12
GPIO_P0_0	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM0	UART2_RX	UART1_CTS	I2C_M0_SCL	SPI1_DI0	SPI1_DCN		JTMS/SWDIO		IR_RX	PDM0_CK	I2S0_DI0	WF_FEM_SW8
GPIO_P0_1	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM1	UART2_TX	UART1_RTS	I2C_M0_SDA	SPI1_DIO			JTCK/SWCK		IR_TX	PDM0_D	I2S0_DO0	WF_FEM_SW9
GPIO_P0_2	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM2	UART1_RX	UART0_CTS	I2C_M1_SCL	SPI1_CS0	SPI1_DI1	SPDIF_DI	JTDI	DISPLAY_BL_EN	IR_RX	PDM1_D	I2S0_WS	WF_FEM_SW1
GPIO_P0_3	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM3	UART1_TX	UART0_RTS	I2C_M1_SDA	SPI1_CLK	SPI1_DI2	SPDIF_DO	JTDO	DISPLAY_BL_PWM	IR_TX	PDM2_D	I2S0_SCK	WF_FEM_SW7
GPIO_P0_4	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM4	UART3_RX	UART1_CTS	I2C_M0_SCL	SPI0_DI0	SPI1_DI3	I2S_MCLK	CLK_OUT	SPI0_DCN	SDMMC_DATA7	PDM1_CK	I2S0_DO3	WF_FEM_SW4
GPIO_P0_5	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM5	UART3_TX	UART1_RTS	I2C_M0_SDA	SPI0_CLK	SPI1_CS1	DISPLAY_SPI_CLK	JRST	DISPLAY_TE	SDMMC_DATA6	PDM0_D	I2S0_DO2	WF_FEM_SW5
GPIO_P0_6	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM6	UART3_RX	UART2_CTS	I2C_M1_SCL	SPI0_CS0	SPI1_CS2	DISPLAY_SPI_CS	WF_SDIO_IRQ	IR_RX	SDMMC_DATA5	PDM1_D	I2S0_DO1	
GPIO_P0_7	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM7	UART3_TX	UART2_RTS	I2C_M1_SDA	SPI0_DIO	SPI1_CS3	DISPLAY_SPI_DIO	SPDIF_DO	IR_TX	SDMMC_DATA4	PDM2_D	I2S0_DO0	
GPIO_P1_0	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM0	UART1_RX	UART2_CTS	I2C_M2_SCL	SPI1_CLK	SPI0_CS1	DISPLAY_SPI_DO1/DC	IR_RX	WF_SDIO_CK	SDMMC_DATA2	SPDIF_DI	I2S0_DI3	
GPIO_P1_1	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM1	UART1_TX	UART2_RTS	I2C_M2_SDA	SPI1_CS0	SPI0_CS2	DISPLAY_SPI_DO2	IR_TX	WF_SDIO_CMD	SDMMC_DATA3	SPDIF_DO	I2S0_DI2	
GPIO_P1_2	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM2	UART2_RX	UART3_CTS	I2C_M2_SCL	SPI1_CS1	SPI0_CS3	DISPLAY_SPI_DO3	CLK_32K_IN	WF_SDIO_D0	SDMMC_CMD	IR_RX	I2S0_DI1	WF_FEM_SW2
GPIO_P1_3	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM3	UART2_TX	UART3_RTS	I2C_M2_SDA	SPI1_DCN	SPI0_DI1	I2S_MCLK	CLK_OUT	WF_SDIO_D1	SDMMC_CLK	IR_TX	I2S0_DI0	WF_FEM_SW3
GPIO_P1_4	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM4	UART2_RX	UART1_CTS	I2C_M1_SCL	SPI1_DI0	SPI0_DI2	DISPLAY_SPI_DI	FLAG_EXC_M33	WF_SDIO_D2	SDMMC_DATA0	IR_RX	DISPLAY_TE	WF_FEM_SW0
GPIO_P1_5	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM5	UART2_TX	UART1_RTS	I2C_M1_SDA	SPI1_DIO	SPI0_DI3	I2S_MCLK	CLK_OUT	WF_SDIO_D3	SDMMC_DATA1	IR_TX	DISPLAY_TE	WF_FEM_SW6
GPIO_P1_6	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM6	UART0_RX	UART3_CTS	I2C_M0_SCL					WF_SDIO_IRQ	BT_UART_RX			
GPIO_P1_7	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM7	UART0_TX	UART3_RTS	I2C_M0_SDA						BT_UART_TX			
GPIO_P2_0	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM0	UART1_RX	UART0_CTS	I2C_M0_SCL	SPI1_DI0	SPI1_DCN	I2S_MCLK	CLK_OUT	WF_UART_RX	BT_UART_RX	SPDIF_DI	I2S1_DI0	WF_FEM_SW0
GPIO_P2_1	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM1	UART1_TX	UART0_RTS	I2C_M0_SDA	SPI1_DIO	IR_TX	DISPLAY_TE	CLK_OUT	WF_UART_TX	BT_UART_TX	SPDIF_DO	I2S1_DO0	WF_FEM_SW6
GPIO_P2_2	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM2	UART2_RX	UART1_CTS	I2C_M1_SCL	SPI1_CS0	DISPLAY_BL_EN	I2S_MCLK	CLK_OUT	WF_UART_CTS	BT_UART_CTS	IR_RX	I2S1_WS	WF_FEM_SW2
GPIO_P2_3	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM3	UART2_TX	UART1_RTS	I2C_M1_SDA	SPI1_CLK	SPI0_DCN	DISPLAY_BL_PWM	PCM_DI	WF_UART_RTS	BT_UART_RTS	CLK_OUT	I2S1_SCK	WF_FEM_SW3
GPIO_P2_4	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM4	UART3_RX	UART0_CTS	I2C_M2_SCL	SPI0_DI0	SPI0_DI3	SPI0_DCN	PCM_DO	SPDIF_DI	WF_SDIO_CK	CLK_REQ_OUT	I2S1_DO3	WF_FEM_SW4
GPIO_P2_5	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM5	UART3_TX	UART0_RTS	I2C_M2_SDA	SPI0_DIO	SPI0_CS3	DISPLAY_TE	PCM_FSYNC	FLAG_EXC_M33	WF_SDIO_CMD	CLK_REQ_IN	I2S1_DO2	WF_FEM_SW5
GPIO_P2_6	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM6	UART3_RX	UART2_CTS	I2C_M0_SCL	SPI0_CS0	SPI1_DI1	CLK_32K_IN	PCM_CLK	IR_RX	WF_SDIO_D0	SPDIF_DI	I2S1_DO1	WF_FEM_SW1
GPIO_P2_7	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM7	UART3_TX	UART2_RTS	I2C_M0_SDA	SPI0_CLK	SPI1_CS1	I2S_MCLK	CLK_OUT	IR_TX	WF_SDIO_D1	SPDIF_DO	I2S1_DO0	WF_FEM_SW9
GPIO_P3_0	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM0	UART1_RX	UART0_RTS	I2C_M1_SCL	SPI0_DI0	SPI1_DI2	SPI0_DCN	WF_UART_RX	SPI1_CS1	WF_SDIO_D2	PDM0_D	I2S1_DI3	WF_FEM_SW0
GPIO_P3_1	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM1	UART1_TX	UART0_CTS	I2C_M1_SDA	SPI0_DIO	SPI1_CS2	DISPLAY_SPI_DI	WF_UART_TX	IR_RX	WF_SDIO_D3	PDM1_D	I2S1_DI2	WF_FEM_SW6
GPIO_P3_2	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM2	UART1_RX	UART3_CTS	I2C_M2_SCL	SPI0_CS0	SPI1_CS3	DISPLAY_SPI_DO3	WF_UART_CTS	IR_TX	WF_SDIO_IRQ	PDM2_D	I2S1_DI1	WF_FEM_SW2
GPIO_P3_3	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM3	UART1_TX	UART3_RTS	I2C_M2_SDA	SPI0_CLK	SPI1_DI3	DISPLAY_SPI_DO2	WF_UART_RTS	SPI1_DCN	DISPLAY_TE	PDM2_CK	I2S1_DI0	WF_FEM_SW3
GPIO_P3_4	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM4	UART3_RX	UART2_CTS	I2C_M0_SCL	SPI1_DI0	SPI0_DI1	DISPLAY_SPI_DO1/DC	CLK_OUT	SPI1_DCN	IR_RX	PDM0_CK	I2S0_DI3	WF_FEM_SW4
GPIO_P3_5	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM5	UART3_TX	UART2_RTS	I2C_M0_SDA	SPI1_DIO	SPI0_CS1	DISPLAY_SPI_DIO	CLK_32K_IN	FLAG_EXC_M33	IR_TX	PDM0_D	I2S0_DI2	WF_FEM_SW5
GPIO_P3_6	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM6	UART2_RX	UART3_CTS	I2C_M2_SCL	SPI1_CS0	SPI0_DI2	DISPLAY_SPI_CS	CLK_REQ_OUT	SPDIF_DI	IR_RX	PDM1_D	I2S0_DI1	WF_FEM_SW7
GPIO_P3_7	Pull up/ Pull down	AVDDIO	no pull	I/O	PWM7	UART2_TX	UART3_RTS	I2C_M2_SDA	SPI1_CLK	SPI0_CS2	DISPLAY_SPI_CLK	CLK_REQ_IN	SPDIF_DO	IR_TX	PDM2_D	I2S0_DI0	WF_FEM_SW8

LED1	Pull up/ Pull down	3.0V(Internal)	Pull up	O	PWM
LED2	Pull up/ Pull down	3.0V(Internal)	Pull up	O	PWM

POWKEY	Pull down	VBAT	Pull down	I

7. Electrical Specifications

7.1 Absolute Maximum Ratings[Note4]

Symbol	Description	Min.	Typ.	Max.	Unit
T_A	Ambient Temperature	-30		80	℃
V_{BAT}	Supply Voltage			6	V
V_{IN}	Input Voltage	-0.3		VDDIO+0.3	V
I_{IN}	Input Current	-10		10	mA
V_{LNA}	LNA Input Level			0	dBm

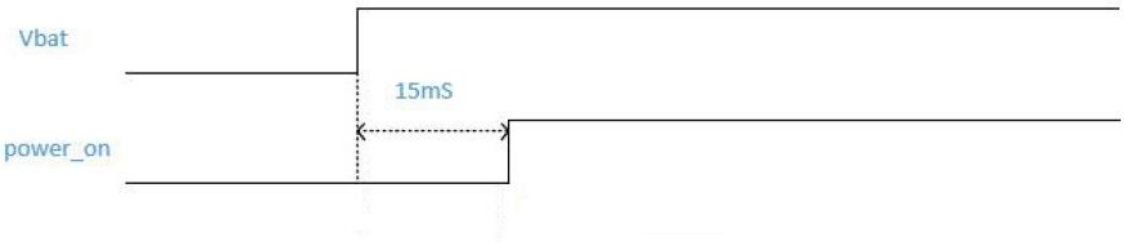
Note4: Stresses beyond those listed absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operations of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit
T_A	Ambient Temperature	-20	25	80	℃
V_{BAT}	Supply Voltage	3.1	3.8	5.5	V
V_{IL}	CMOS Low Level Input Voltage	0		0.3*VDDIO[Note5]	V
V_{IH}	CMOS High Level Input Voltage	0.7*VDDIO		VDDIO	V
V_{OL}	Low level Output Voltage			0.1*VDDIO	V
V_{OH}	High level Output Voltage	0.9*VDDIO			V
V_{TH}	CMOS Threshold Voltage		0.5*VDDIO		V

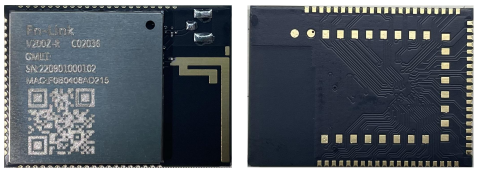
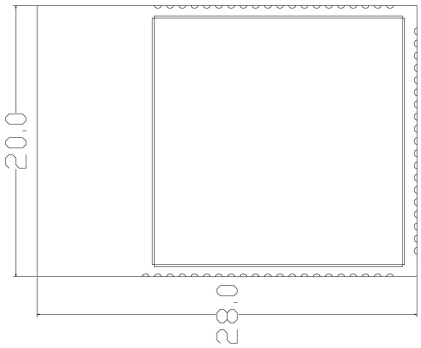
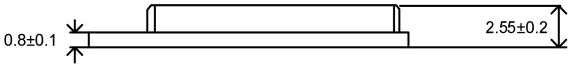
Note5: VDDIO=3.3V by default.

7.3 Power up sequence



8. Size reference

8.1 Module Picture

<table>
<tr><td>L: 28 (+0.3/-0.1) mm
W: 20 (+/-0.1)mm
  </td><td> 
</td></tr>
<tr><td>H: 2.55 (±0.2) mm</td><td> 
</td></tr>
<tr><td>Weight</td><td>2.2g</td></tr>
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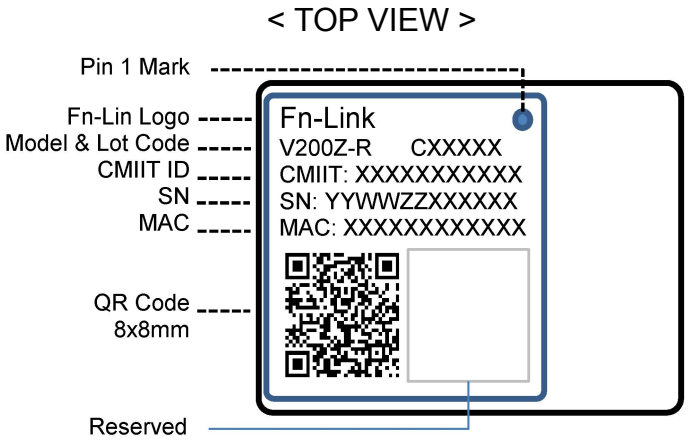
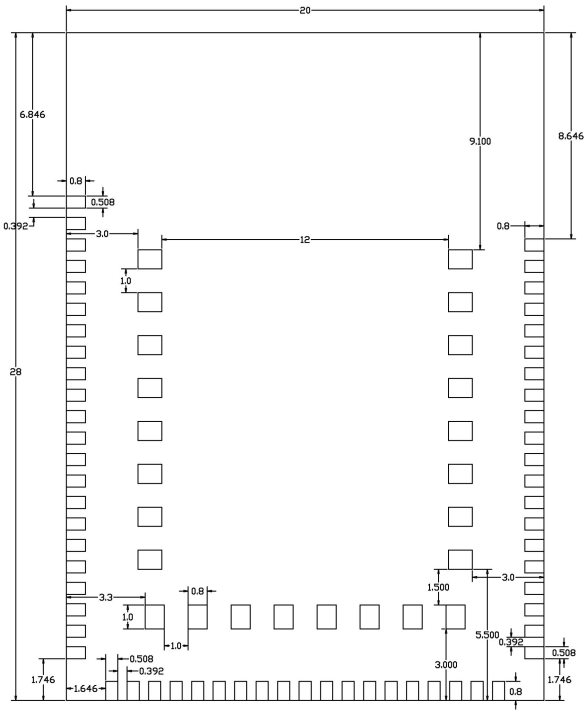
8.2 Marking Description



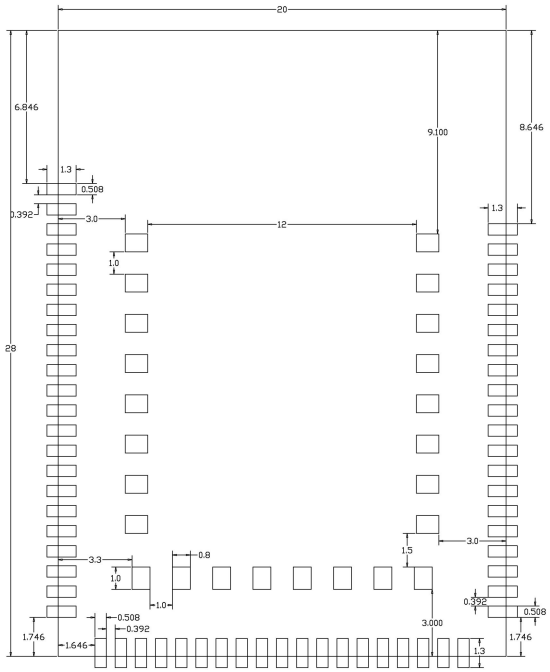
8.3 Physical Dimensions

<TOP View>



8.4 Layout Recommendation

<TOP View>



9. The Key Material List

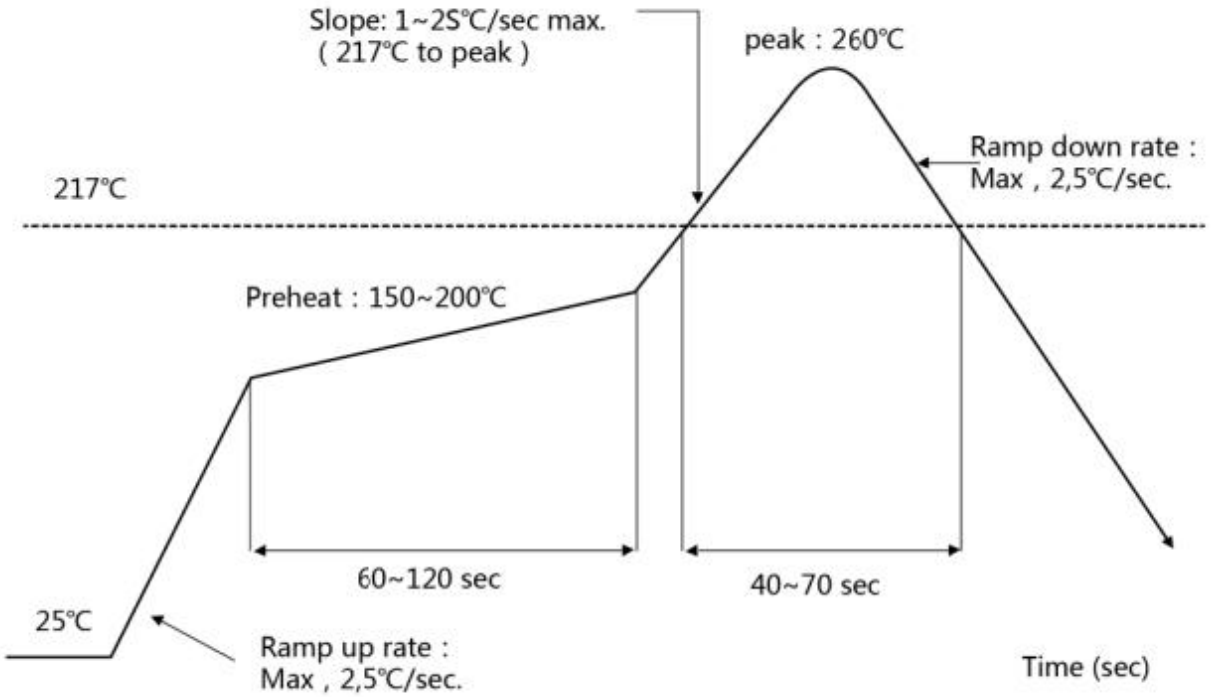
Chipset	BES2600, BGA-169L, 6.6x6.8mm, Pitch 0.5mm	Bestechnic
PCB	V200Z-R, 28X20X0.8mm, 4L HDI, Matte black	Brain-power, KX-PCB, SL-PCB, Sunlord
Crystal	3225, 24MHz, 10ppm	TST,HOSONIC,TKD,ECEC,JWT
Inductor	2520, 2.2uH ,±20%	Sunlord, Cenke, Ceaiya, Microgate
Shielding	V200Z-R, Shielding cover, 18.5x18.6x1.7mm, T=0.2mm	Suntech, JLT

10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260°C

Number of Times : ≤2 times



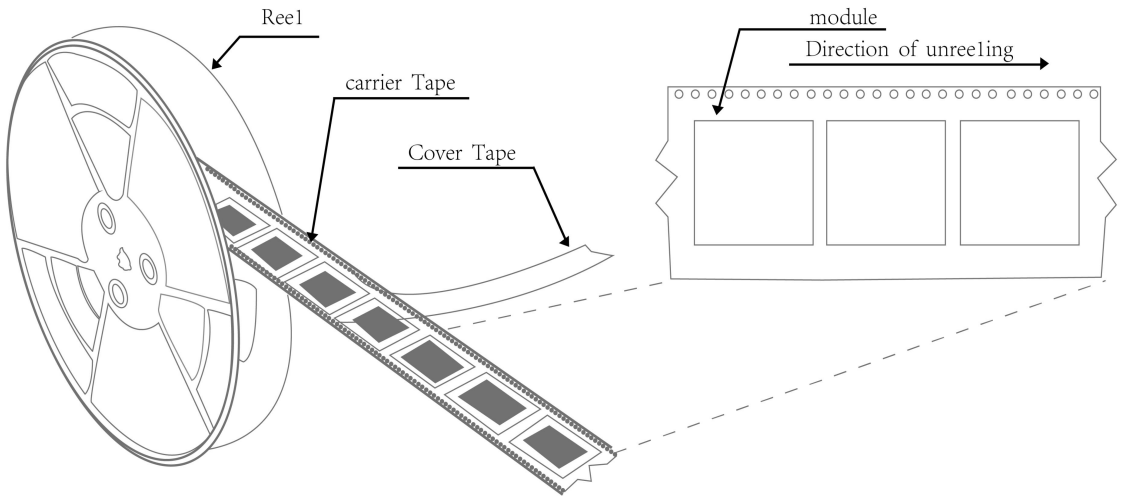
11. RoHS compliance

All hardware components are fully compliant with EU RoHS directive

12. Package

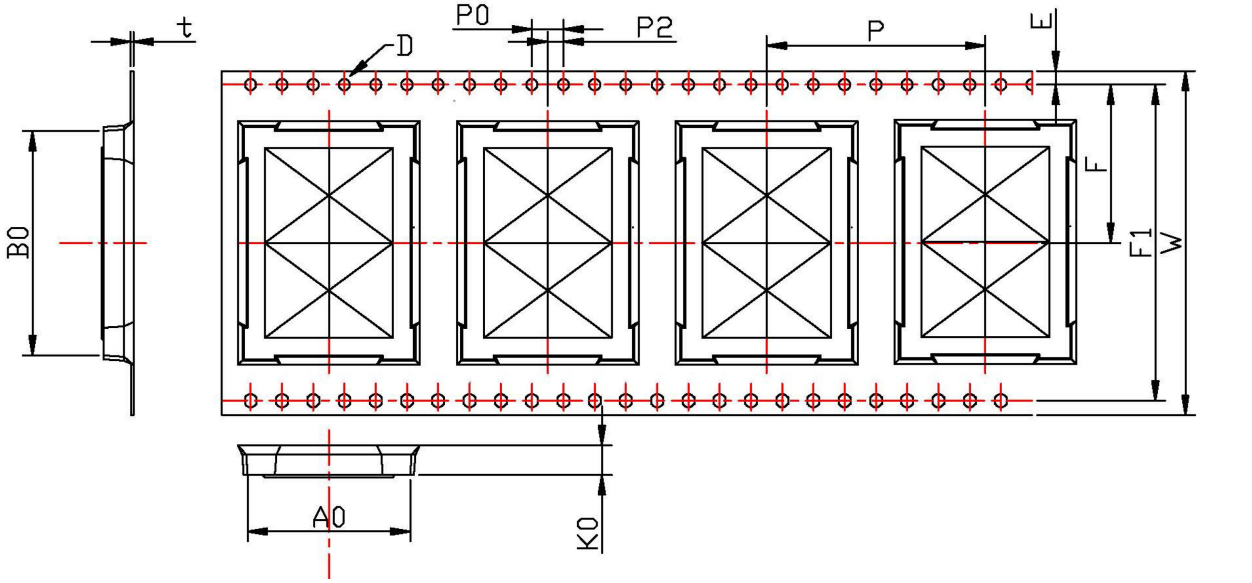
12.1 Reel

A roll of 500pcs



12.2 Carrier Tape Detail

ITEM	W	A0	B0	D	E	F	F1	K0	P0	P2	P	T
DIM	44	20.40	28.35	1.5	1.75	20.2	40.4	3.80	4.0	2.0	28.0	0.30
TOLE	+0.3 -0.3	±0.15	±0.15	+0.1 -0.0	±0.1	±0.15	±0.10	±0.10	±0.1	±0.15	±0.1	±0.05



12.3 Packaging Detail

the take-up package

Using self-adhesive tape

Width of black tape: 44mm the cover tape :37.5mm

Color of plastic disc: blue

NY bag size:500mm*420mm size ： 335X335X55mm

The packing case size:360*210*370mmg

13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

d) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

e) Baking is required if conditions b) or c) are not respected

f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more