FN-LINK欧智通

PRODUCT SPECIFICATION

J102T-RR

Wi-Fi Single-band 1x1 802.11b/g/n + BLE5.0 Combo Module

Version:v1.1

J102T-RR Module Datasheet

Ordering Information	Part No.	Description
	FGJ102TRRX-00	BL602C-00-Q2I,b/g/n Wi-Fi/BLE 1T1R,16x24mm, on-board antenna

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

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Contents

Revision History

Version	Date	Description	Draft	Checked	Approved
V1.0	2021/03/4	New Version	Fc		
V1.1	2022/09/01	Modify the definition of an I/O port	Zzq		

1. General Description

1.1 Introduction

The J102T-RR is a Wi-Fi + BLE combination chipset for low power and high performance application development. The wireless subsystem contains 2.4G radio, Wi-Fi 802.11b/g/n and BLE 5.0 baseband /MAC designs. The microcontroller subsystem contains a low-power 32-bit RISC CPU, cache, and memory. The power management unit controls the low power mode. In addition, various security features are supported.

1.2 Description

Modal Name	J102T-RR
Product Description	Support Wi-Fi/BLE functionalities
Dimension	L x W x H: 16 x 24 x 2.85 mm
Wi-Fi Interface	Support UART
BT Interface	UART
Operating temperature	-20°C to 85°C
Storage temperature	-40°C to 125°C

2. Features

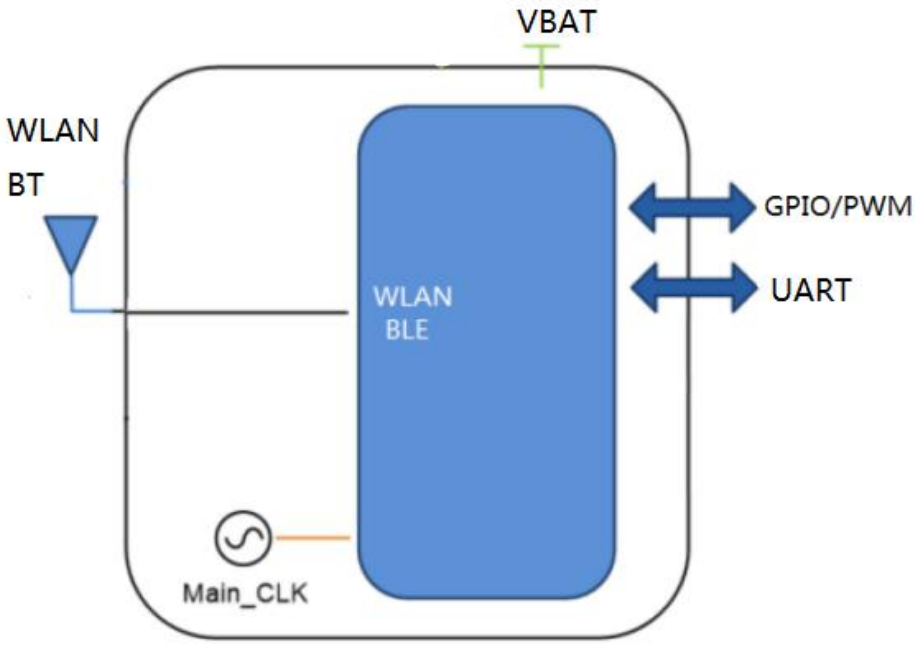
General

- Supports IEEE 802.11b /g/n protocol.
- 2.4GHz band 1T1R mode, support 20 MHz, data rate up to 72.2 Mbps.
- Wi-Fi securit WPS/WEP/WPA/WPA2 Personal/WPA2Enterprise/WPA3.
- Supports Station + BLE mode and Station + SoftAP + BLE mode.
- Wi-Fi and BLE coexist.

Bluetooth Features

- Bluetooth low energy5.0, Bluetooth Mesh
- BLE assists with fast Wi-Fi connections.
- Support BLE 5.0 channel choice # 2.

3. Block Diagram



4. General Specification

4.1 2.4GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n/ac/ax Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.497 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 18dBm ± 2 dB	EVM ≤ -9dB
	802.11g /54Mbps : 14dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 14dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps @ -92 dBm	≤-83 dBm
	- 11Mbps @ -85 dBm	≤-76 dBm
Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps @ -89 dBm	≤-85 dBm
	- 54Mbps @ -70 dBm	≤-68 dBm
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 @ -89 dBm	≤-85 dBm
	- MCS=7 @ -68 dBm	≤-67 dBm
Maximun Input Level	802.11b : -10 dBm	
	802.11g/n : -20 dBm	

4.2 Bluetooth Specification

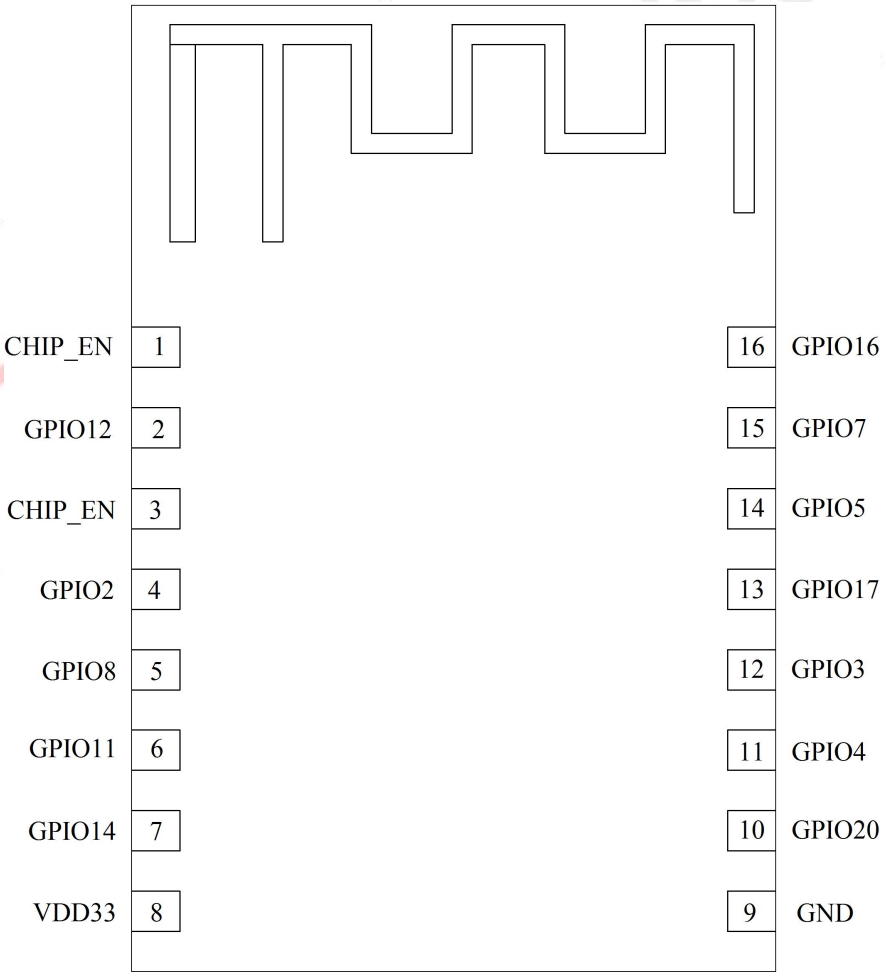
Feature	Description
General	
Bluetooth	Bluetooth V5.0
Interface	UART
Frequency Range	2402 MHz ~ 2480 MHz
Number od Channels	79 channels
RF Specification	

	Min(dBm)	**Typical**(dBm)	**Max**(dBm)
Output Power (Class 1)	0	5	15
Sensitivity @ BER=0.1% for GFSK (1Mbps)			-70
Maximun Input Level	GFSK (1Mbps):-20dBm		

5. Pin Definition

5.1 Pin Outline

< TOP VIEW >



5.2 Pin Definition Details

NO.	Name	Type	Description	Voltage
1	CHIP_EN	I	Power enable of module ON: pull high ; OFF: pull low	
2	GPIO12	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	
3	CHIP_EN	I	Power enable of module ON: pull high ; OFF: pull low	
4	GPIO2	I/O	Connect FLASH , NC	VDDIO
5	GPIO8	I/O	Boot strap selection.Pin state sampled on rising edge of CHIP_EN. High: Boot from interface. Low: Boot from flash.	
6	GPIO11	I/O	GPIO Pin. Chip Jtag TDO pin，Not recommended	
7	GPIO14	—	GPIO Pin. The MUX Function can be referred to Pin Function Table	VDDIO
8	VDD33	—	3.3V Input	3.3V
9	GND	-	Ground connections	
10	GPIO20		Connect FLASH , NC	
11	GPIO4	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	VDDIO
12	GPIO3	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	VDDIO
13	GPIO17	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	VDDIO
14	GPIO5	I/O	GPIO Pin. The MUX Function can be referred to Pin Function Table	VDDIO
15	GPIO7	I	GPIO Pin/UART RX	VDDIO
16	GPIO16	O	GPIO Pin/UART TX	VDDIO

P:POWER I:INPUT O:OUTPUT VDDIO: 3.3V

Download：3.3V，GPIO7,GPIO16,GND,GPIO8 Pull up before the module is powered on.

RFTest：3.3V，GPIO7,GPIO16,GND,GPIO8 suspended or drop down.

5.3 Pin Function Group Table

Pin Name	Flash[1]	SDIO	SPI (Default /SWAP=1)	UART[2](Default /SWAP=1)	I2C Master	PWM	Analog	External_PA	JTAG (Default /SWAP=1)	IR
PAD_GPIO_0	SF2_D1	CLK	MOSI /MISO	SIG0 /SIG4	SCL	PWM_CH0	-	FEM0	TMS/TCK	-
PAD_GPIO_1	SF2_D2	CMD	MISO /MOSI	SIG1 /SIG5	SDA	PWM_CH1	-	FEM1	TDI/TDO	-
PAD_GPIO_2	SF2_D3	DAT0	SS	SIG2 /SIG6	SCL	PWM_CH2	-	FEM2	TCK/TMS	-
PAD_GPIO_3	-	DAT1	SCLK	SIG3 /SIG7	SDA	PWM_CH3	-	FEM3	TDO/TDI	-
PAD_GPIO_4	-	DAT2	MOSI /MISO	SIG4 /SIG0	SCL	PWM_CH4	ADC_CH1	FEM0	TMS/TCK	-
PAD_GPIO_5	-	DAT3	MISO /MOSI	SIG5 /SIG1	SDA	PWM_CH0	ADC_CH4	FEM1	TDI/TDO	-
PAD_GPIO_6	-	-	SS	SIG6 /SIG2	SCL	PWM_CH1	ADC_CH5	FEM2	TCK/TMS	-
PAD_GPIO_7	-	-	SCLK	SIG7 /SIG3	SDA	PWM_CH2	-	FEM3	TDO/TDI	-
PAD_GPIO_8	-	-	MOSI /MISO	SIG0 /SIG4	SCL	PWM_CH3	-	FEM0	TMS/TCK	-
PAD_GPIO_9	-	-	MISO /MOSI	SIG1 /SIG5	SDA	PWM_CH4	ADC_CH6/7	FEM1	TDI/TDO	-
PAD_GPIO_10	-	-	SS	SIG2 /SIG6	SCL	PWM_CH0	MICBIAS /ADC_CH8/9	FEM2	TCK/TMS	-
PAD_GPIO_11	-	-	SCLK	SIG3 /SIG7	SDA	PWM_CH1	ADC_CH10 /IRTX	FEM3	TDO/TDI	IRRX (ir_rx_gpio_sel=1)
PAD_GPIO_12	-	-	MOSI /MISO	SIG4 /SIG0	SCL	PWM_CH2	ADC_CH0	FEM0	TMS/TCK	IRRX (ir_rx_gpio_sel=2)
PAD_GPIO_13	-	-	MISO /MOSI	SIG5 /SIG1	SDA	PWM_CH3	ADC_CH3 /DAC_A	FEM1	TDI/TDO	IRRX (ir_rx_gpio_sel=3)
PAD_GPIO_14	-	-	SS	SIG6 /SIG2	SCL	PWM_CH4	ADC_CH2 /DAC_B	FEM2	TCK/TMS	-
PAD_GPIO_15	-	-	SCLK	SIG7 /SIG3	SDA	PWM_CH0	psw_irrcv_out /ADC_CH11	FEM3	TDO/TDI	-
PAD_GPIO_16	-	-	MOSI /MISO	SIG0 /SIG4	SCL	PWM_CH1	-	FEM0	TMS/TCK	-
PAD_GPIO_17	SF1_D3	-	MISO /MOSI	SIG1 /SIG5	SDA	PWM_CH2	-	FEM1	TDI/TDO	-
PAD_GPIO_18	SF1_D2	-	SS	SIG2 /SIG6	SCL	PWM_CH3	-	FEM2	TCK/TMS	-
PAD_GPIO_19	SF1_D1	-	SCLK	SIG3 /SIG7	SDA	PWM_CH4	-	FEM3	TDO/TDI	-

Pin Name	Flash[1]	SDIO	SPI (Default /SWAP=1)	UART[2](Default /SWAP=1)	I2C Master	PWM	Analog	External_PA	JTAG (Default /SWAP=1)	IR
PAD_GPIO_20	SF1_D0 /SF2_D0	-	MOSI /MISO	SIG4 /SIG0	SCL	PWM_CH0	-	FEM0	TMS/TCK	-
PAD_GPIO_21	SF1_CS /SF2_CS	-	MISO /MOSI	SIG5 /SIG1	SDA	PWM_CH1	-	FEM1	TDI/TDO	-
PAD_GPIO_22	SF1_CLK /SF2_CLK	-	SS	SIG6 /SIG2	SCL	PWM_CH2	-	FEM2	TCK/TMS	-
PAD_GPIO_23	SF0_CLK	-	-	-	-	-	-	-	-	-
PAD_GPIO_24	SF0_CS	-	-	-	-	-	-	-	-	-
PAD_GPIO_25	SF0_D0	-	-	-	-	-	-	-	-	-
PAD_GPIO_26	SF0_D1	-	-	-	-	-	-	-	-	-
PAD_GPIO_27	SF0_D2	-	-	-	-	-	-	-	-	-
PAD_GPIO_28	SF0_D3	-	-	-	-	-	-	-	-	-

6. Electrical Specifica tions

6.1 Power Supply DC Characteristics

	MIN	TYP	MAX	Unit
Operating Temperature	-20	25	85	deg.C
VCC33	3.0	3.3	3.6	V
VDDIO	3.0	3.3	3.6	V

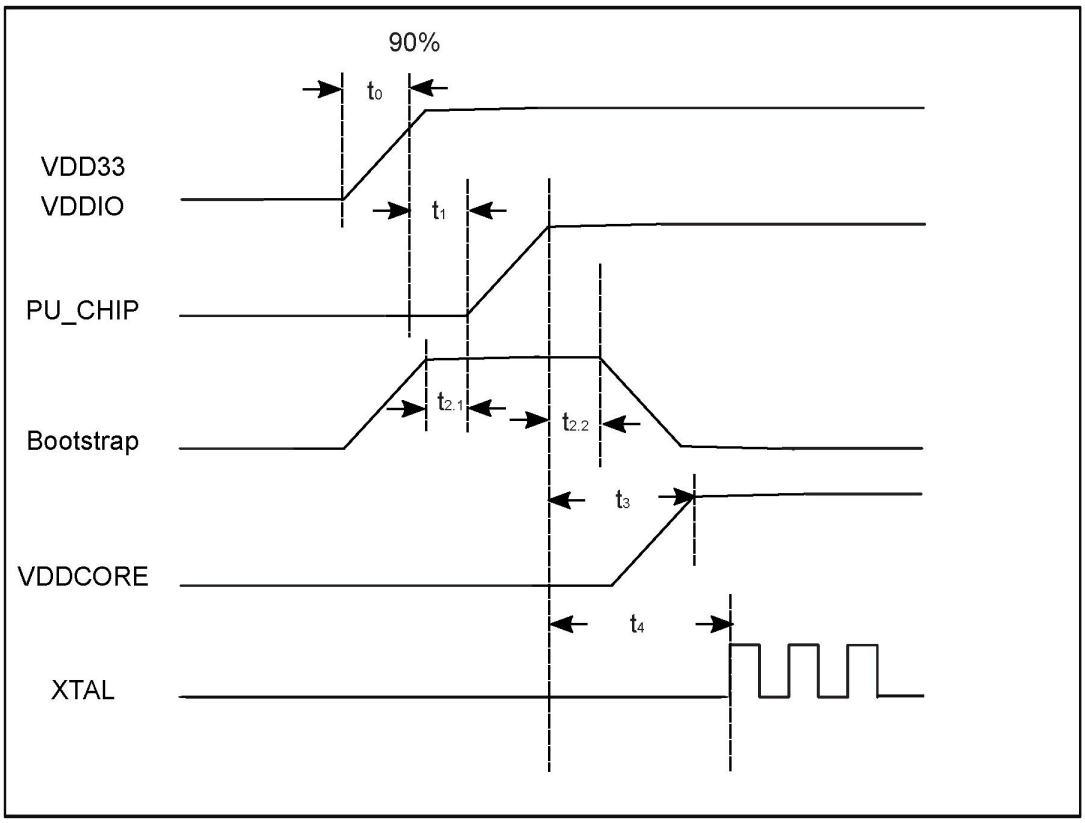
6.2 Power Consumption

Mode		Note	Performance @3.3Vdc 25◦C			
			Min.	Typ	Max.	Unit
RX	11b			35		mA
	11g			39		
	11n			39		
	BLE 1Mbps	Duty 60%		31		
TX	11b - 11Mbps @21dBm	Duty 50%		190		
		Duty 99%		310		
	11g - 54Mbps @18dBm	Duty 50%		145		
		Duty 99%		230		
	11n - MCS7 @17dBm	Duty 50%		130		
		Duty 99%		215		
	BLE 1Mbps @15dBm	Duty 86%		133		

6.3 Power-on Sequence

6.3.1 Power-on Sequence

To ensure normal power-on and startup, the power supply, reset, and Bootstrap pins must meet the corresponding power-on sequence requirements.

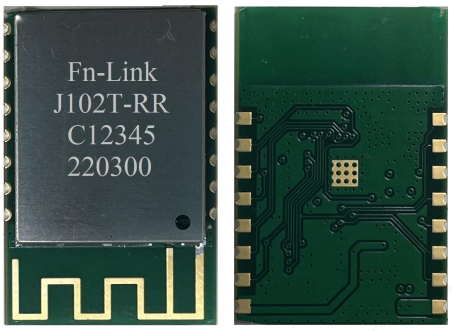
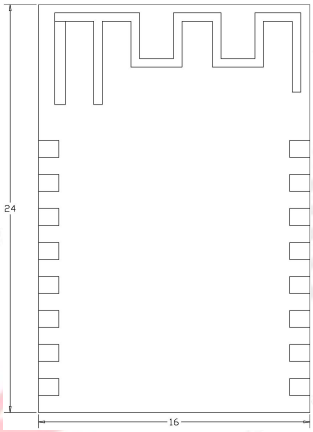
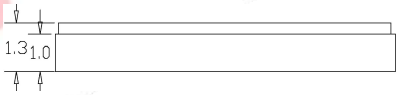


Param	Description	Min.(ms)	Typical	Max.(ms)
t_0	The rise time when the supply voltage reaches 90%			2
t_1	Delay before the power supply is raised until the PU_CHIP is raised.	0.1		
$t_{2.1}$	Boostrap pin[1] level is set up before the PU_CHIP is pulled up.	0		
$t_{2.2}$	Hold the Boostrap pin level after the PU_CHIP is pulled up.	2		
t_3	PU_CHIP pulls up to VDDCORE output		2	
t_4	PU_CHIP pulls high until XTAL starts vibrating		2	

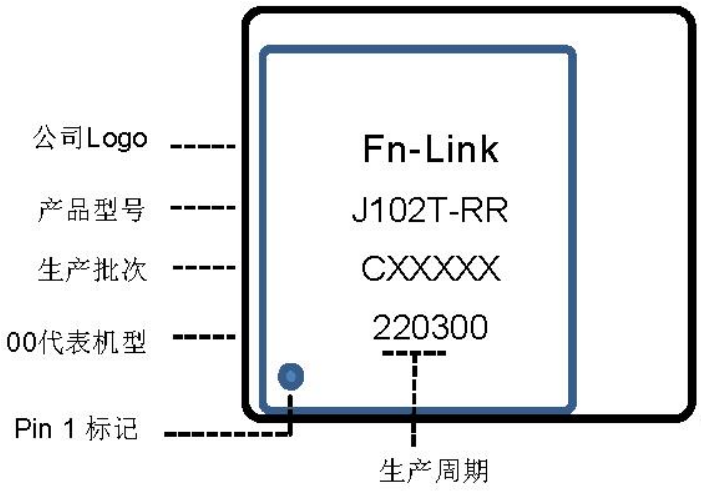
[1] Bootstrap pin is GPIO8.

7. Size Reference

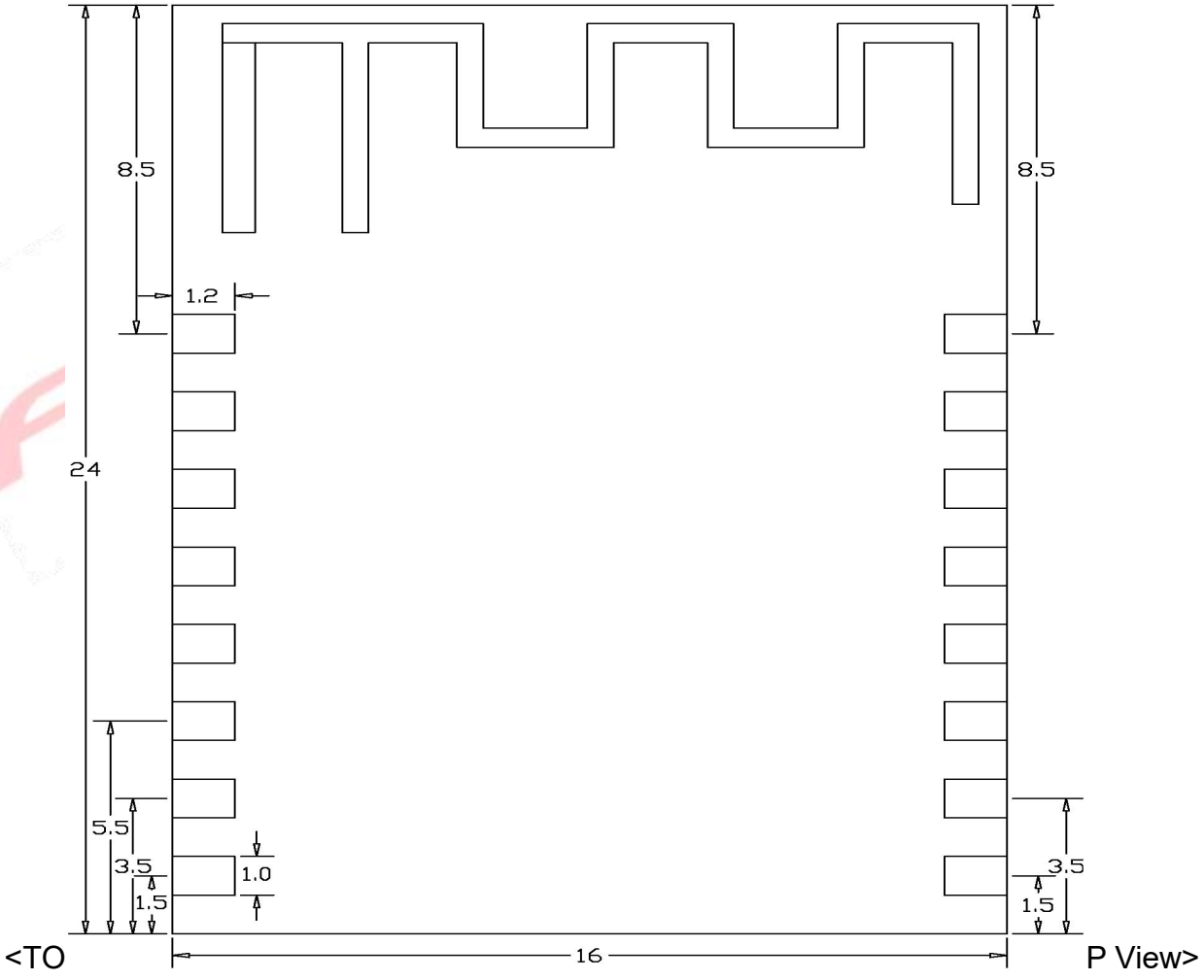
7.1 Module Picture

<table>
<tr><td>L x W : 16 x 24 (+0.3/-0.1) mm
 
</td><td> 
</td></tr>
<tr><td>H: 2.85 (±0.2) mm</td><td> 
</td></tr>
<tr><td>Weight</td><td>1.6g</td></tr>
</table>

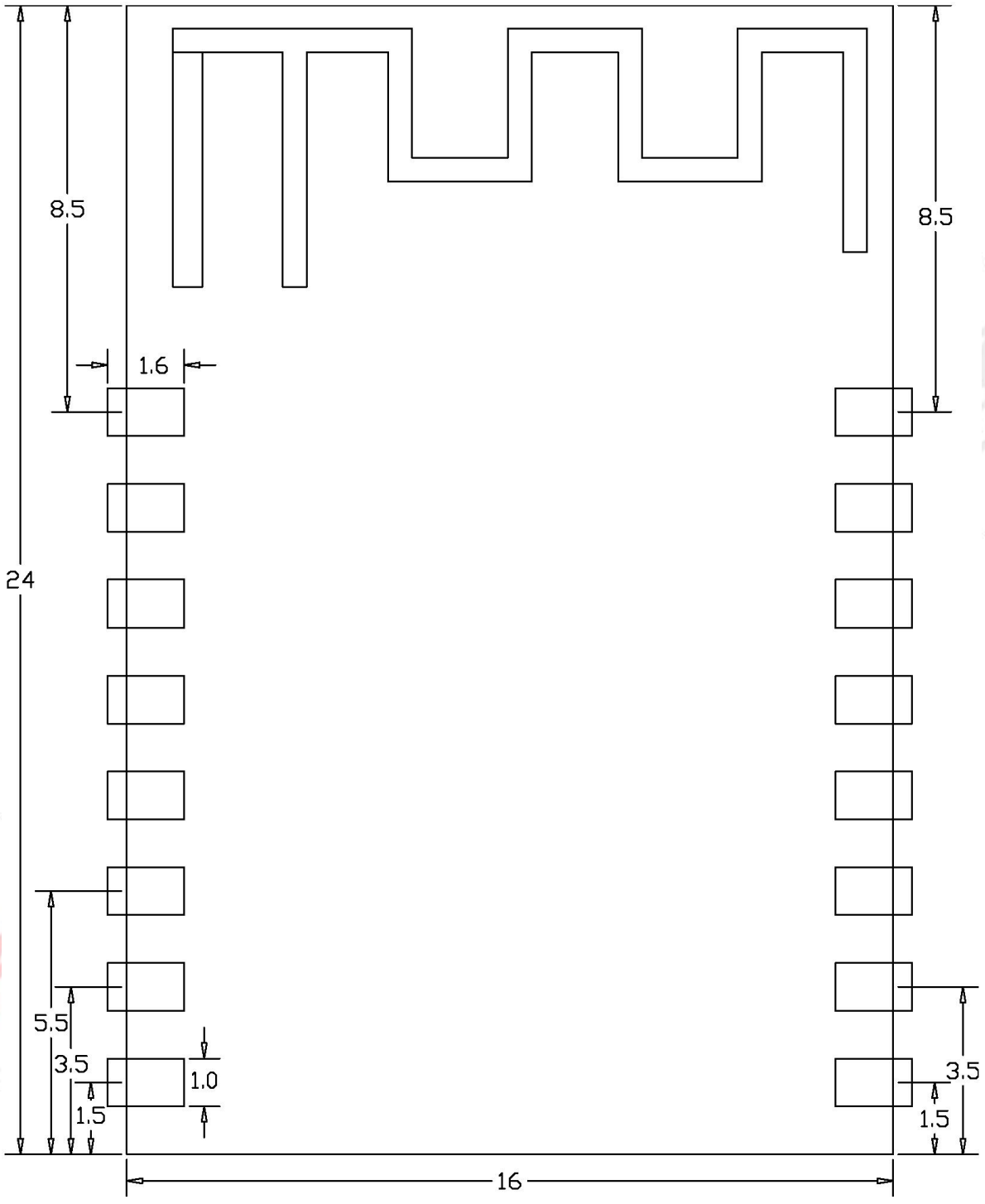
7.2 Marking Description



7.3 Physical Dimension



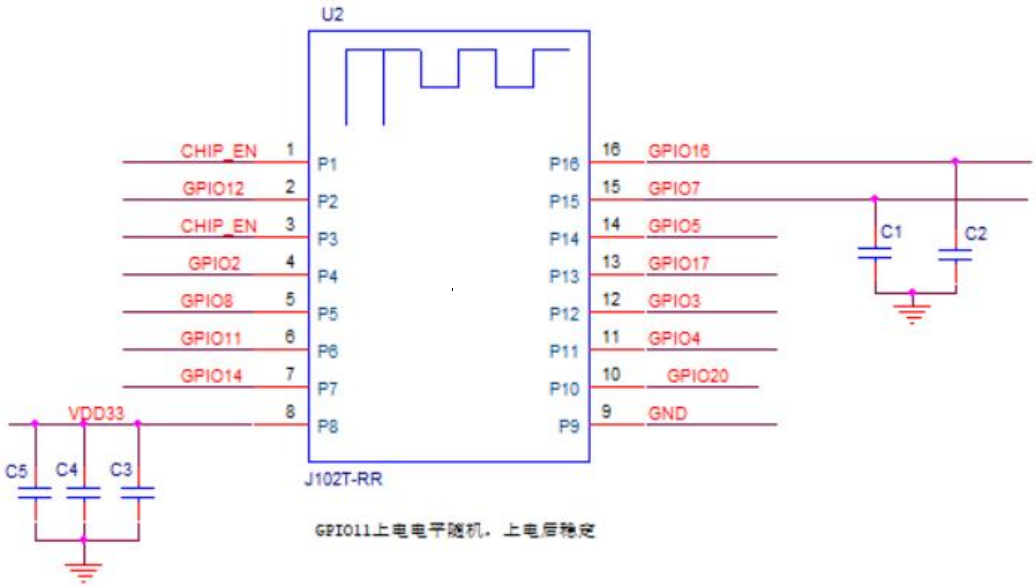
7.4 Layout Recommendation



8. The Key Material List

Items	Part Name	Description	Manufacturer
1	Crystal	3225 40MHz ±10ppm,12pF	ECEC, TKD, Hosonic, JWT, TXC
2	Chipset	BL602C-00-Q2I QFN32	Bouffalo Lab
3	PCB	J102T-RR 4L,FR4,16*24*1.0mm	XY-PCB,GDKX,Sunlord, SL-PCB
4	Shielding	J102T-RR Shielding	信太，精力通

9. Reference Design



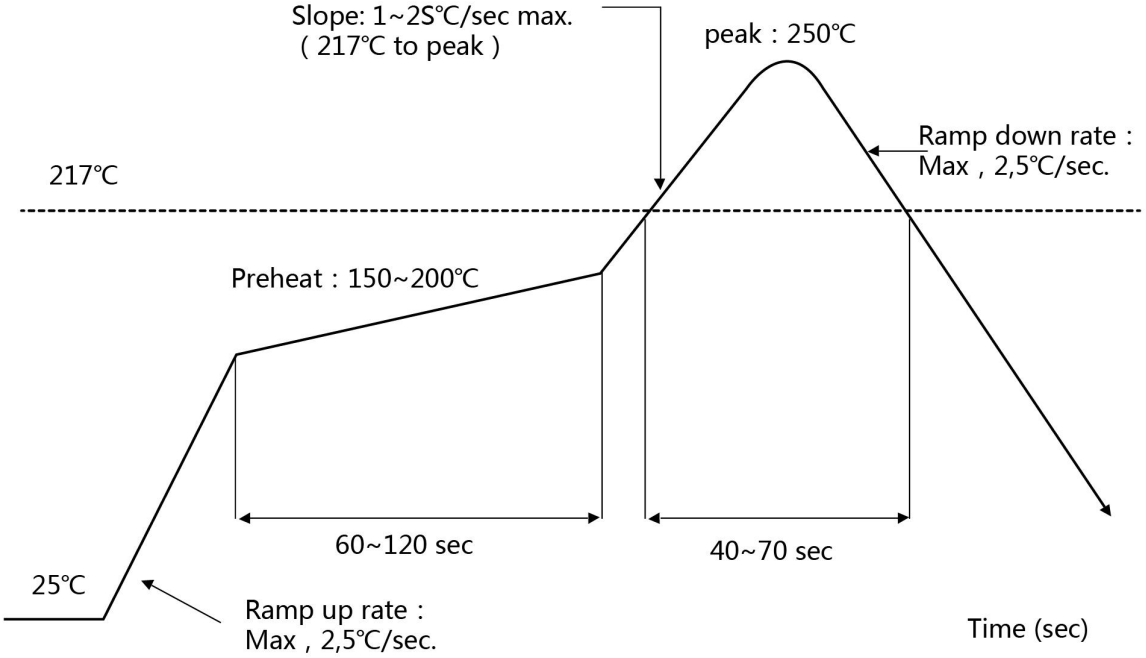
10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature: 250±5 °C

5Time within 5° C of peak temperature：≥10s

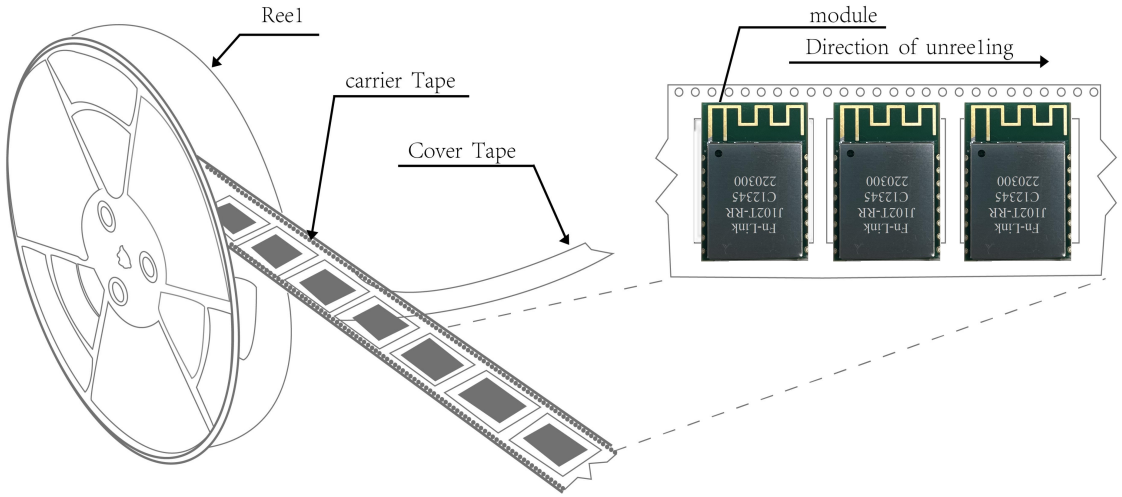
Number of Times: 2 times



11. Package

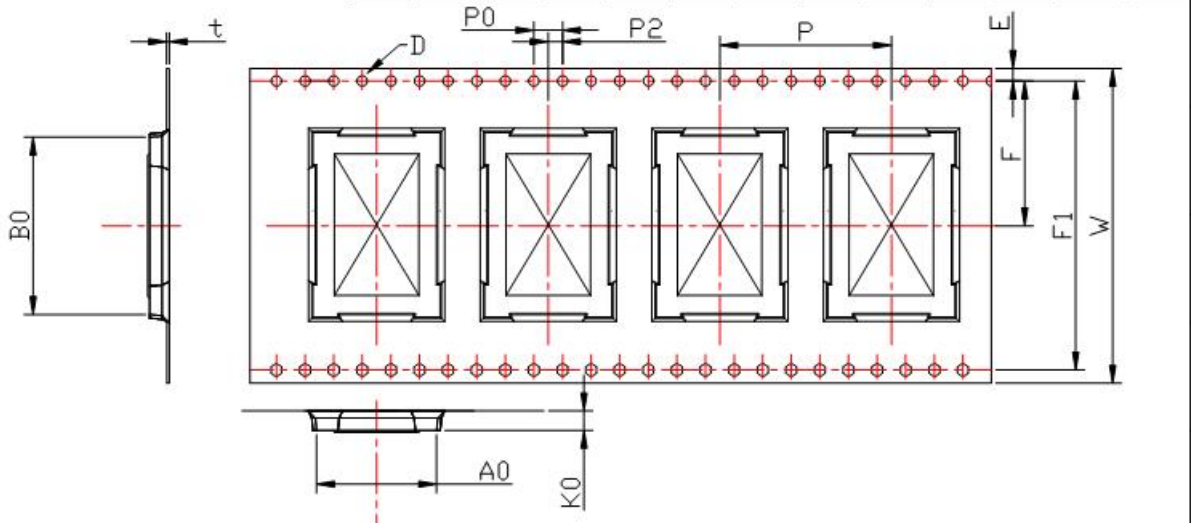
11.1 Reel

A roll of 860pcs



11.2 Carrier Tape Detail

ITEM	W	A0	B0	D	E	F	F1	K0	P0	P2	P	T
DIM	44	16.40	24.40	1.5	1.75	20.2	40.4	2.80	4.0	2.0	24.0	0.30
TOLE	+0.3 -0.3	±0.15	±0.15	+0.1 -0.0	±0.1	±0.15	±0.10	±0.10	±0.1	±0.15	±0.1	±0.05



11.3 Packaging Detail

The take-up package:

Using self-adhesive tape
Color of plastic disc: blue

NY bag size: 500mm*420mm

Internal box size: 350X350X55mm

Carton size: 360X210X370mm

12. Moisture Sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

d) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

e) Baking is required if conditions b) or c) are not respected

f) Baking is required if the humidity indicator inside the bag indicates 10% RH or more