FN-LINK 欧智通

PRODUCT SPECIFICATION

8274N-PR

Wi-Fi Dual-band 2x2 11ac + Bluetooth 5.0

Combo Module

Version:v1.1

8274N-PR Module Datasheet

Ordering Information	Part NO.	Description
	FG8274NPRX-00	QCA6574A-1, a/b/g/n/ac Wi-Fi+BLE5.0, 2T2R, 23.4X19.4mm, PCIE+ Uart(车规)

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

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Revision History

Version	Date	Contents of Revision Change	Preparde	Checked	Approved
V1.0	2021/10/21	New version	-	LXY	QJP
V1.1	2022/10/15	change tolerance to ±2db Update the specification format Added '车规'标识	LXY	LXY	QJP

1. General Description

1.1 Introduction

8274N-PR is a single-die WLAN and BT combo module. support 2×2 MIMO with two spatial streams IEEE802.11 a/b/g/n/ac WLAN standards and Bluetooth 5.0 enabling seamless integration of WLAN/Bluetooth and Low Energy technology. Supports low power PCIe (w/L1 sub-state) interfaces for WLAN and UART/PCM interface for Bluetooth.

1.2 Description

Model Name	8274N-PR
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 23.4 x 19.4 x 2.3 mm
Wi-Fi Interface	PCI-e
BT Interface	UART / PCM
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	-40° C to 85° C
Storage temperature	-40° C to 125° C

2. Features

General

- Highly integrated WLAN SOC for 5 GHZ 802.11ac, or 2.4G/5G 802.11n WLAN applications .
- Maximal Likelihood (ML) decoding, Low-Density Parity Check(LDPC), Rx Space Time Block Code (STBC), and 1.5 kb of On Chip One-time Programmable (OTP) memory.
- Supports 20 MHz/40 MHz at 2.4 GHz and supports 20 MHz/40MHz/80 MHz at 5 GHz.

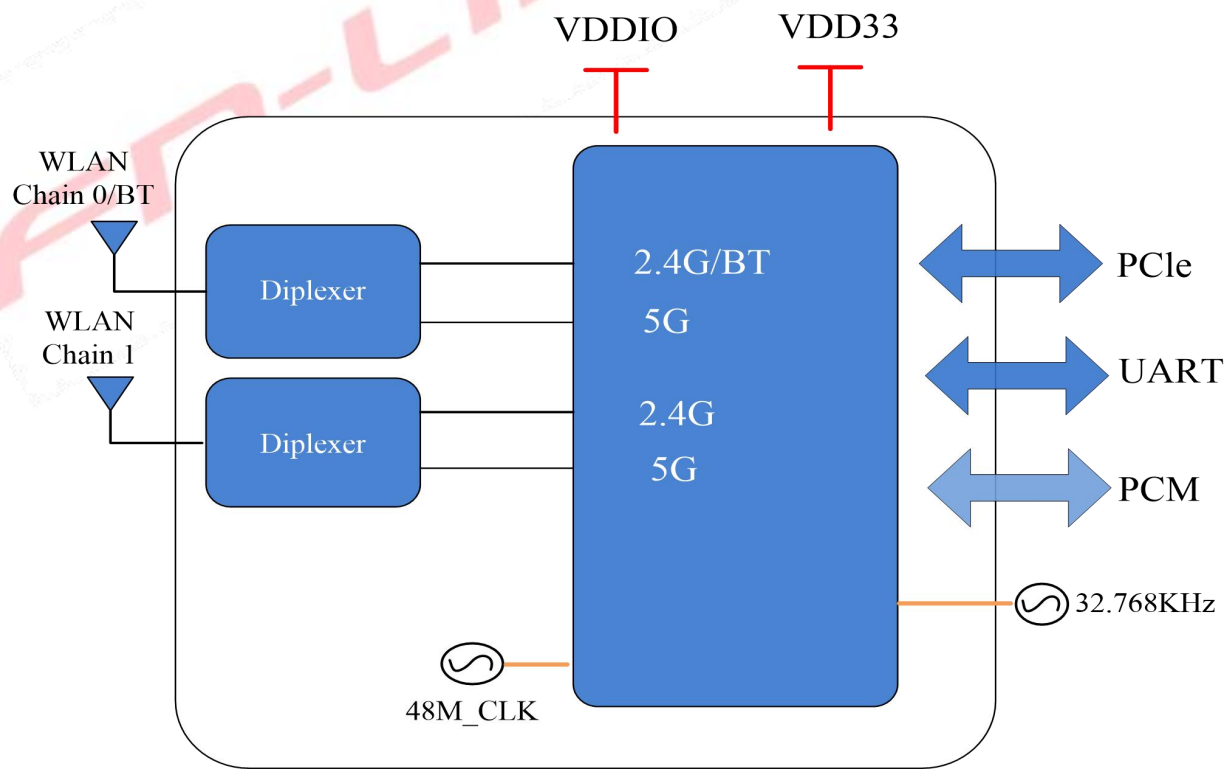
Host Interface

- Supports Bluetooth-WLAN coexistence and ISM-LTE coexistence.

Bluetooth Features

- Supports Bluetooth 5.0, ANT+ and is backward-compatible with previous Bluetooth versions from v1.2 .
- BT host digital interface:
  - HCI UART (up to 3.2 Mbps)
  - PCM for audio data

3. Block Diagram



4. General Specification

4.1 2.4GHz WI-FI Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz：Ch1 ~ Ch14	
Test Items	**Typical Value**	**EVM**
Output Power	802.11b /11Mbps : 16dBm ± 2 dB	EVM ≤ -9dB
	802.11g /54Mbps : 14dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 13dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps PER @ -92 dBm, typical	≤-90
	- 11Mbps PER @ -85 dBm, typical	≤-78
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps PER @ -89 dBm, typical	≤-84
	- 54Mbps PER @ -71 dBm, typical	≤-67
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -89 dBm, typical	≤-84
	- MCS=7 PER @ -69 dBm, typical	≤-66
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 PER @ -86 dBm, typical	≤-81
	- MCS=7 PER @ -67 dBm, typical	≤-63
Maximum Input Level	802.11b : -10 dBm	
	802.11g/n : -20 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

4.2 5GHz WI-FI Specification

Feature	Description	
WLAN Standard	IEEE 802.11 a/n/ac, Wi-Fi compliant	
Frequency Range	5.150 GHz ~ 5.850 GHz (5.0 GHz Band)	
Number of Channels	5.0GHz：Please see the table[1]	
Test Items	**Typical Value**	**EVM**

Output Power	802.11a /54Mbps : 10dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 9dBm ±2 dB	EVM ≤ -28dB
	802.11ac /MCS9 : 5dBm ±2 dB	EVM ≤ -32dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	±20ppm	
SISO Receive Sensitivity (11a,20MHz) @10% PER	- 6Mbps PER @ -88 dBm, typical	≤-84
	- 54Mbps PER @ -70 dBm, typical	≤-67
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -88 dBm, typical	≤-84
	- MCS=7 PER @ -68 dBm, typical	≤-66
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0 PER @ -85 dBm, typical	≤-81
	- MCS=7 PER @ -67 dBm, typical	≤-63
SISO Receive Sensitivity (11ac,20MHz) @10% PER	- MCS=0, NSS1 PER @ -86 dBm, typical	≤-82
	- MCS=8, NSS1 PER @ -67 dBm, typical	≤-60
SISO Receive Sensitivity (11ac,40MHz) @10% PER	- MCS=0, NSS1 PER @ -84 dBm, typical	≤-79
	- MCS=9, NSS1 PER @ -62 dBm, typical	≤-55
SISO Receive Sensitivity (11ac,80MHz) @10% PER	- MCS=0, NSS1 PER @ -81 dBm, typical	≤-78
	- MCS=9, NSS1 PER @ -56 dBm, typical	≤-53
Maximum Input Level	802.11a/n : -30 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

[1]5GHz(20MHz) Channel table

Band range	Operating Channel Numbers	Channel center frequencies(MHz)
5180MHz~5240MHz	36	5180
	40	5200
	44	5220
	48	5240
5260MHz~5320MHz	52	5260
	56	5280
	60	5300
	64	5320
5550MHz~5700MHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640
	132	5660
	136	5680
	140	5700
5745MHz~5825MHz	149	5745

	153	5765
	157	5785
	161	5805
	165	5825

Note: output power may updated in future version.

4.3 Bluetooth Specification

Feature	**Description**		
General Specification			
Bluetooth Standard	Bluetooth V5.0		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	GFSK, π/4-DQPSK, 8-DPSK		
RF Specification			
	Min(dBm)	**Typical**(dBm)	**Max**(dBm)
Output Power (Class 1)	3	10	15
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-91	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-90	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-85	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	π/4-DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

5. ID setting information

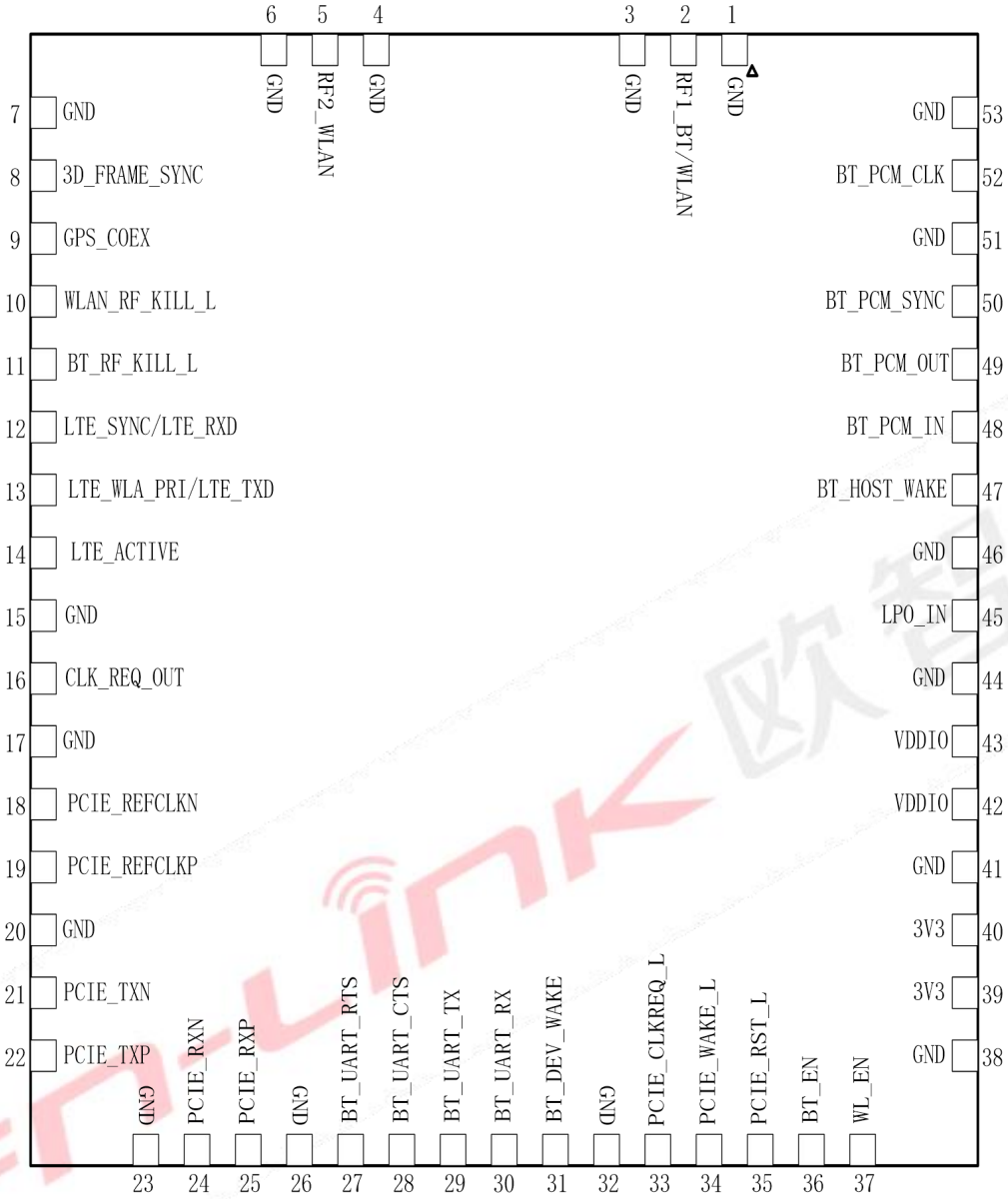
WI-FI

Vendor ID	-
Product ID	-

6. Pin Definition

6.1 Pin Outline

< TOP VIEW



6.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND	—	Ground connection	
2	RF1_BT/WLAN	I/O	WL_BT_ANT0 RF output	
3	GND	—	Ground connection	
4	GND	—	Ground connection	

5	RF2_WLAN	I/O	WL_ANT1 RF output	
6	GND	—	Ground connection	
7	GND	—	Ground connection	
8	3D_FRAME_SYNC	I/O	Frame sync signal from TV to sync with 3D glass viaBluetooth.NC if not used	VDDIO
9	GPS_COEX	I/O	GPS co-existence signal. High means WLAN is in transmit.NC if not used	VDDIO
10	WLAN_RF_KILL_L	I	Turn-off WLAN RF analog and frontend. Active low. NC if not used	VDDIO
11	BT_RF_KILL_L	I	Turn-off Bluetooth RF analog and front-end. Active low.NC if not used	VDDIO
12	LTE_SYNC/LTE_RXD	I/O	LTE co-existence signal.LTE_UART_RXD or LTE_FS.NC if not used	VDDIO
13	LTE_WLA_PRI/LTE_TXD	I/O	LTE co-existence signal. LTE_UART_TXD or LTE_PRI.NC if not used	VDDIO
14	LTE_ACTIVE	I/O	LTE co-existence signal (it is not required if using 2-wire interface for LTE co- existence.NC if not used	VDDIO
15	GND	—	Ground connection	
16	CLK_REQ_OUT	O	Clock request output.NC if not used	VDDIO
17	GND	—	Ground connection	
18	PCIE_REFCLKN	I	PCI-E CLK Difference -(100MHz)	
19	PCIE_REFCLKP	I	PCI-E CLK Difference +(100MHz)	
20	GND	—	Ground connection	
21	PCIE_TXN	O	PCI-E Data OUT Difference -	
22	PCIE_TXP	O	PCI-E Data OUT Difference +	
23	GND	—	Ground connection	
24	PCIE_RXN	I	PCI-E Data IN Difference -	
25	PCIE_RXP	I	PCI-E Data IN Difference +	
26	GND	—	Ground connections	
27	BT_UART_RTS	I/O	BT UART interface	VDDIO
28	BT_UART_CTS	I/O	BT UART interface	VDDIO
29	BT_UART_RX	I	BT UART interface	VDDIO
30	BT_UART_TX	O	BT UART interface	VDDIO
31	BT_DEV_WAKE	I	Host wakeupBluetooth, active high.NC if not used	VDDIO

32	GND	—	Ground connections	
33	PCIE_CLKREQ_L	O	Reference clock request.	VDDIO
34	PCIE_WAKE_L	O	Request to service a function-initiated wake event	VDDIO
35	PCIE_RST_L	I	PCI express reset with weak pull-down	VDDIO
36	BT_EN	I	Bluetooth enable signal, active high is low in reset.	VDDIO
37	WL_EN	I	WLAN enable signal, active high is low in reset.	VDDIO
38	GND	—	Ground connection	
39	3V3	P	Main power source input	3.3V
40	3V3	P	Main power source input	3.3V
41	GND	—	Ground connection	
42	VDDIO	P	IO power source input	1.8V/3.3V
43	VDDIO	P	IO power source input	1.8V/3.3V
44	GND	—	Ground connection	
45	LPO_IN	I	External sleep clock input(32.768kHz).	VDDIO
46	GND	—	Ground connections	
47	BT_HOST_WAKE	O	BT wakeupHOST, active high.NC if not used	VDDIO
48	BT_PCM_IN	I	BT PCM interface	VDDIO
49	BT_PCM_OUT	O	BT PCM interface	VDDIO
50	BT_PCM_SYNC	I	BT PCM interface	VDDIO
51	GND	—	Ground connection	
52	BT_PCM_CLK	I/O	BT PCM interface	VDDIO
53	GND	—	Ground connection	

P:POWER I:INPUT O:OUTPUT VDDIO:3.3V

7. Electrical Specifications

7.1 Power Supply DC Characteristics

	Min.	Typ.	Max.	Unit

Operating Temperature	-40	25	85	°C
VDD	3.15	3.3	3.45	V
VDDIO	1.71	1.8 or 3.3	3.45	V

Digital logic characteristics

Parameter		Comments	Min	Typ	Max	Units
V_{IH}	High-level input voltage		0.7 x VDDIO	–	VDDIO+0.3	V
V_{IL}	Low-level input		-0.3	–	0.3 x VDDIO	V
V_{SHYS}	Schmitt hysteresis		-	1.8 V IO: 375 3.3 V IO: 645	–	mV
I_{IL}	Input low leakage current	V_IN = 0 V; supply = VDDIO max	-5.0	–	5.0	µA
V_{OH}	High-level output voltage		0.9 x VDDIO	–	VDDIO	V
V_{OL}	Low-level output voltage		0	–	0.1 x VDDIO	V
I_{OH}	HIgh-level output current		3	–	–	mA
I_{OL}	Low-level output current		–	–	-11	mA
C_{IN}	Input capacitance		–	–	3	pF

Digital pad internal pull resistor

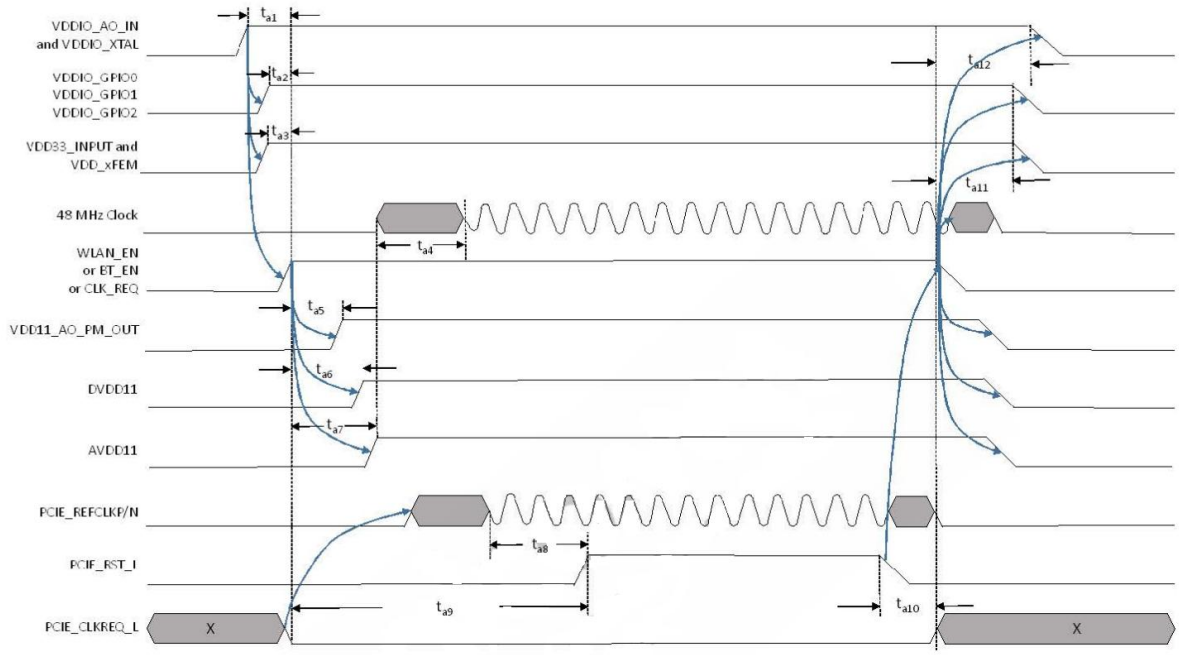
Internal pull resistor	VDDIO = 1.8 V		VDDIO = 3.3 V	
	R (kΩ)		R (kΩ)	
	Min.	Max.	Min.	Max.
Pull down	23	72	24	60
Pull up	70	168	49	95

7.2 Power Consumption

		VCC33 = 3.3V(Unit:mA)
Power Consumption	Wi-Fi on Mode	-
	TX (2.4G 11b mode)	483
	RX (2.4G mode)	110
	TX (5G mode HT80)	642
	RX (5G mode HT80)	237
	BT TX	61
	BT RX	19

7.3 Interface Circuit time series

7.3.1 PCIe powerup sequence timing



QCA6574A-1 power on and power off sequence timing

Symbol	Parameter	Min	Max	Units
t_{a1}	VDDIO_AO valid to WL_EN input active (see Note)	12	–	µs
t_{a2}	VDDIO_XXX valid to WL_EN input active	10	–	µs
t_{a3}	VDD33 valid to WL_EN input active	10	–	µs
t_{a4}	48 MHz clock stabilization time	1	–	ms
t_{a5}	WL_EN valid to AO 1.1 V established	–	500	µs
t_{a6}	WL_EN valid to DVDD11 established	–	3.5	ms
t_{a7}	WL_EN valid to AVDD11 established	–	4	ms
t_{a8}	REFCLK stable before PCIE_RST_L de-assert	100	–	µs
t_{a9}	WL_EN valid to PCIE_RST_L de-assert	10	–	ms
t_{a10}	PCIE_RST_L assert to WL_EN de-assert	10	–	µs
t_{a11}	WL_EN de-assert to VDDIO_XXX and VDD33 ramping down	10	–	µs
t_{a12}	WL_EN de-assert to VDDIO_AO ramping down (see Note)	12	–	µs

NOTE VDDIO_AO must be on at first and off at last, VDDIO_AO must be >1.62 V at all times when VDD33 > 1 V.

PCIe power sequence timing requirements (external 1.1 V)

Symbol	Parameter	Min	Max	Units
t_{b1}	VDDIO_AO valid to WL_EN input active[1,2]	12	–	µs
t_{b2}	VDDIO_XXX valid to WL_EN input active	10	–	µs
t_{b3}	VDD33 valid to WL_EN input active	10	–	µs
t_{b4}	WL_EN valid to VDD11 external 1.1V established	8	–	µs
t_{b5}	48 MHz clock stabilization time	1	–	ms
t_{b6}	WL_EN valid to AO 1.1V established	–	500	µs
t_{b7}	REFCLK stable before PCIE_RST_L de-assert	100	–	µs
t_{b8}	WL_EN valid to PCIE_RST_L de-assert[3]	10	–	µs
t_{b9}	PCIE_RST_L assert to WL_EN de-assert	10	–	µs
t_{b10}	WL_EN de-assert to VDD11 ramping down	8	–	µs
t_{b11}	WL_EN de-assert to VDDIO_XXX and VDD33 ramping down	10	–	µs
t_{b12}	WL_EN de-assert to VDDIO_AO ramping down[1]	12	–	µs

1. VDDIO_AO must be on first and off last. VDDIO_AO must also be >1.62 V at all times when VDD33 > 1V.
2. VDDIO_XTAL may be on before or at the same time as VDDIO_GPIOx. VDDIO_XTAL must not be on before VDDIO_AO.
3. PCIe should enter LTSSM detect state within 20 ms of the end of fundamental reset.

7.3.2 UART timing

UART parameter	Value
Number of data bits	Eight
Parity bit	No parity
Stop bit	One stop bit
Flow control	RTS/CTS (hardware)
Flow off response	Two bytes maximum
Supported transport bit rates (bps) [a]	9.6 K, 19.2 K, 38.4 K, 57.6 K, 115.2 K, 125 K, 230.4 K, 250 K, 460.8 K, 500 K, 720 K, 921.6 K, 1 M, 1.6 M, 2 M, 3 M, 3.2 M, with an accuracy of +1.5/-2.5%
Host baud rate tolerance	±3%

[a] UART maximum baud rate is 3.2 Mbps.

The HCI UART transmit timing is showing in Figure 3-14 and Table 3-30.The HCI UART receive timing is as shown in Figure 3-15 and Table 3-31.

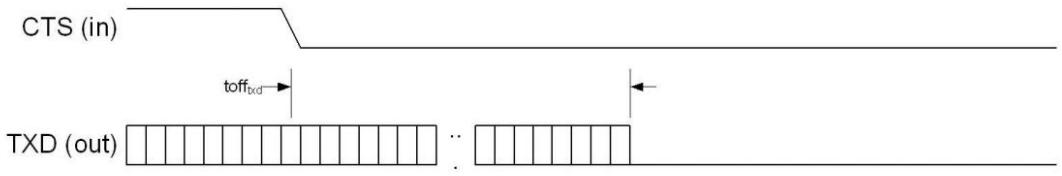


Figure 3-14 HCI UART transmit flow control timing

Table 3-30 HCI UART transmit flow control timing

Parameter	Description	Min	Typ	Max	Unit
$toff_{txd}$	Delay from CTS to TXD stop	—	—	1	byte

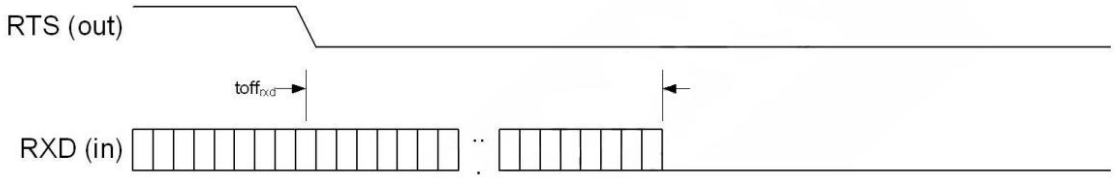


Figure 3-15 HCI UART receive flow control timing

Table 3-31 HCI UART receive flow control timing

Parameter	Description	Min	Typ	Max	Unit
$toff_{rxd}$	Delay from RTS to RXD stop	16	—	—	byte

7.3.3 PCM timing

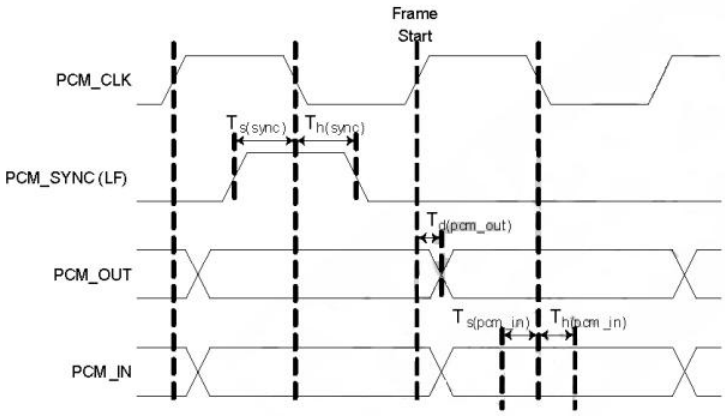


Figure 3-16 PCM interface timing diagram (slave)

Table 3-34 PCM interface timing in slave mode

Symbol	Description	Min	Typ	Max	Units
F_{pcm_clk}	PCM_CLK frequency	64	–	2,048	kHz
Ts_{pcm_sync}	Setup time PCM_SYNC to PCM_CLK fall	0	–	–	ns
Th_{pcm_sync}	Hold time PCM_CLK fall to PCM_SYNC fall	150	–	–	ns
Td_{pcm_out}	Delay from PCM_CLK rise to PCM_OUT	0	–	150	ns
Ts_{pcm_in}	Setup time PCM_IN to PCM_CLK fall	0	–	–	ns
Th_{pcm_in}	Hold time PCM_IN after PCM_CLK fall	150	–	–	ns

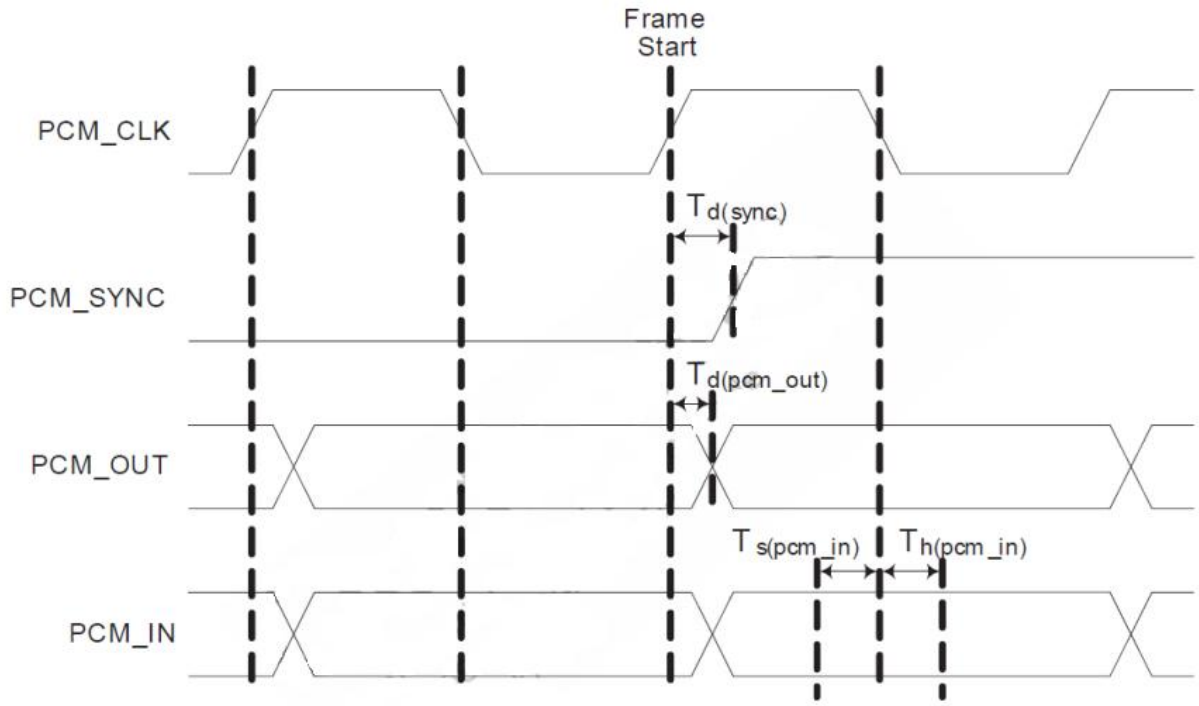


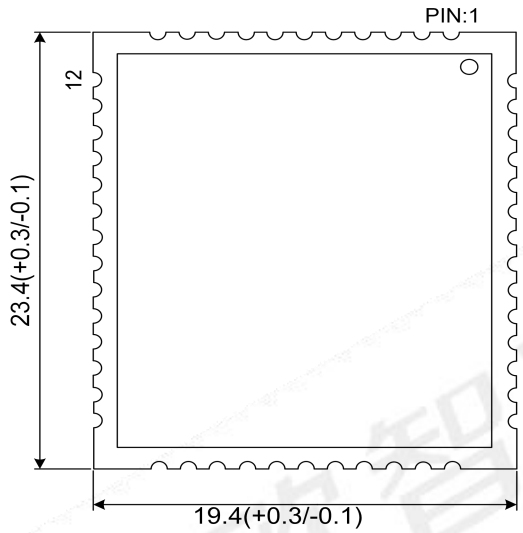
Figure 3-17 PCM interface timing diagram (master)

Table 3-35 PCM interface timing in master mode

Symbol	Description	Min	Typ	Max	Units
F_{pcm_clk}	PCM_CLK frequency	64	–	2048	kHz
Td_{sync}	Delay from PCM_CLK rise to long SYNC	-10	–	50	ns
Td_{pcm_out}	Delay from PCM_CLK rise to PCM_OUT	-10	–	50	ns
Ts_{pcm_in}	Setup time PCM_IN to PCM_CLK fall	50	–	–	ns
Th_{pcm_in}	Hold time PCM_IN after PCM_CLK fall	150	–	–	ns

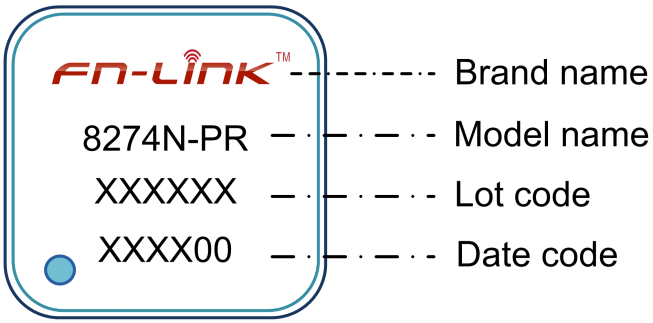
8. Size reference

8.1 Module Picture

L x W :23.4 x 19.4(+0.3/-0.1) mm 	
H: 2.3 (±0.2) mm	
Weight	2.1g

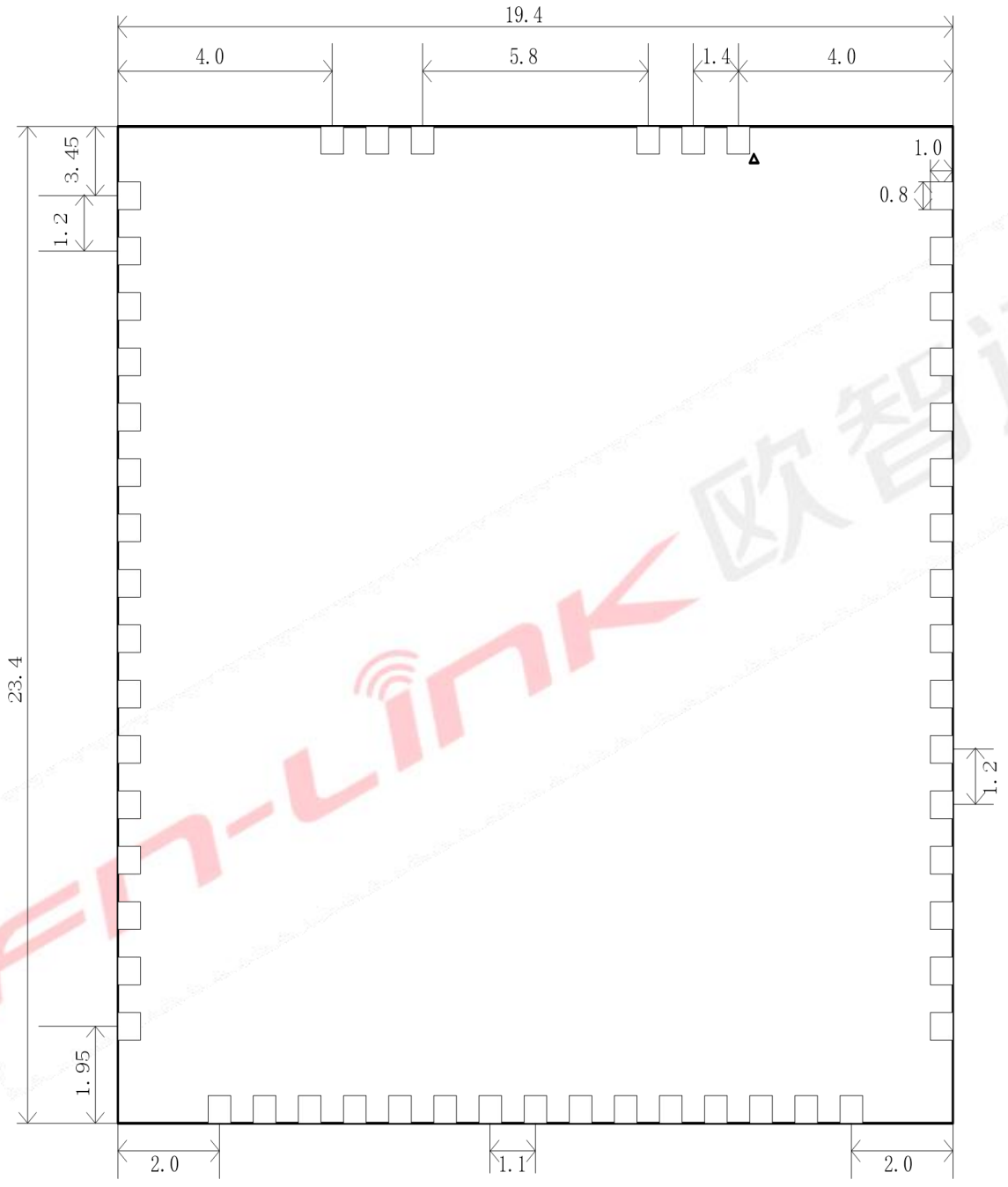
8.2 Marking Description

< TOP VIEW >

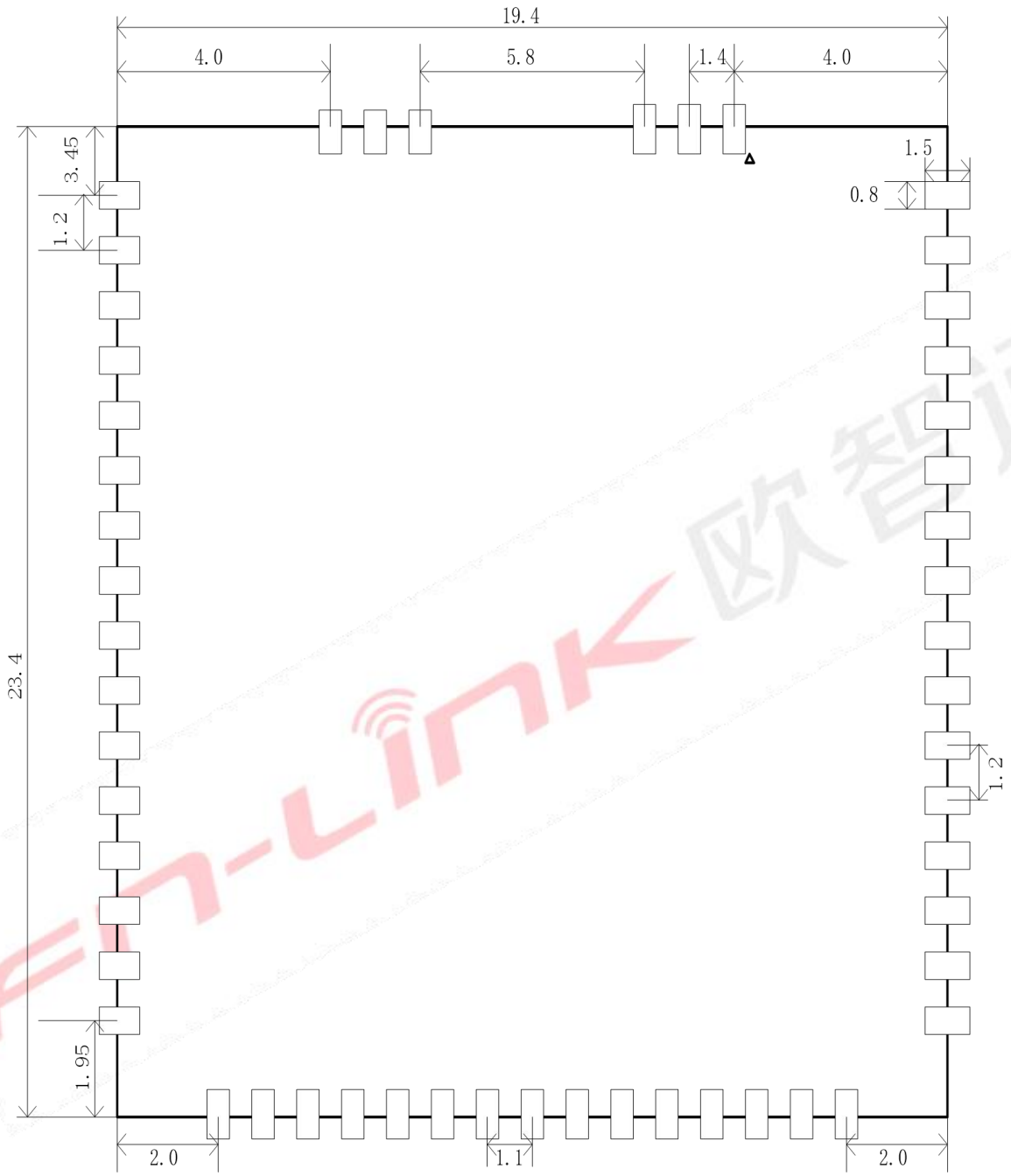


8.3 Physical Dimensions

<TOP View>



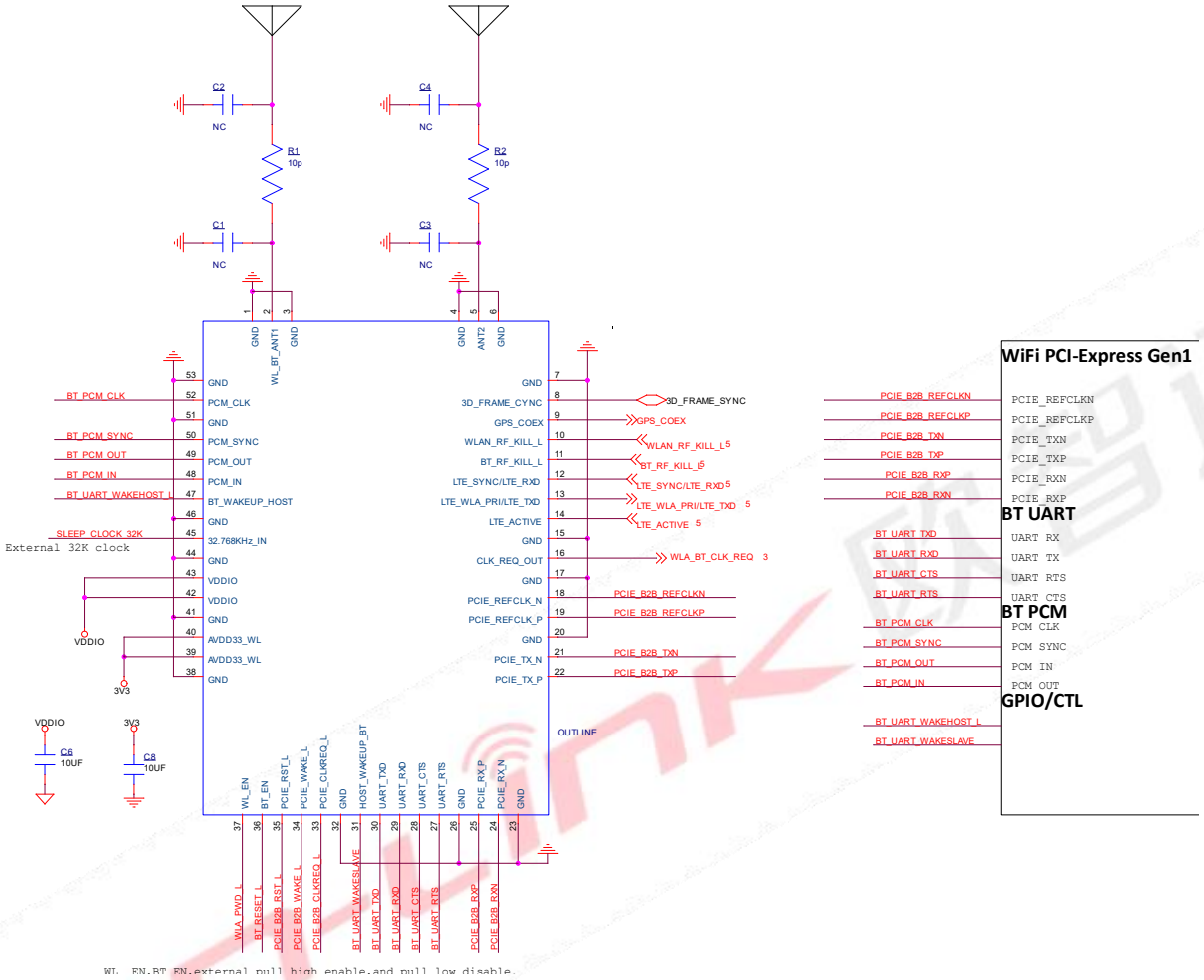
8.4 Layout Recommendation



9. The Key Material List

Diplexer	Diplexers, 1608	ACX,TDK,Walsin,Glead
Filter	BAND PASS FILTER, 2.4G bands	ACX,Walsin,Taiyo,TDK,Glead
Inductor	2016 1.5uH,±20%,138mΩ ,1.2A	Murata,Sunlord,INPAQ,Chilisin ,Ceaiya,Microgate
Shielding cover	8274N-PR shield cover copper	信太，Jlitong,卓益
Crystal	2016 48MHZ 20ppm,12pF	ECEC,TKD,JWT,Hosonic
TVS	0201 5V 0.15pF 12KV	WAYON,Murata,JIEJIE
Chipset	QCA-6574A-1-176CSP-TR-07-0	Qualcomm
Diode	SMPA1345-040LF,SMD 1X0.6-0.5mm	Skyworks，Galaxy
PCB	8274N-PR PCB,6LAYER,FR4,23.4x19.4x0.8mm	kx-pcb,Sunlord,xy-pcb,xl-pcb,b rainpower,truly

10. Reference Design

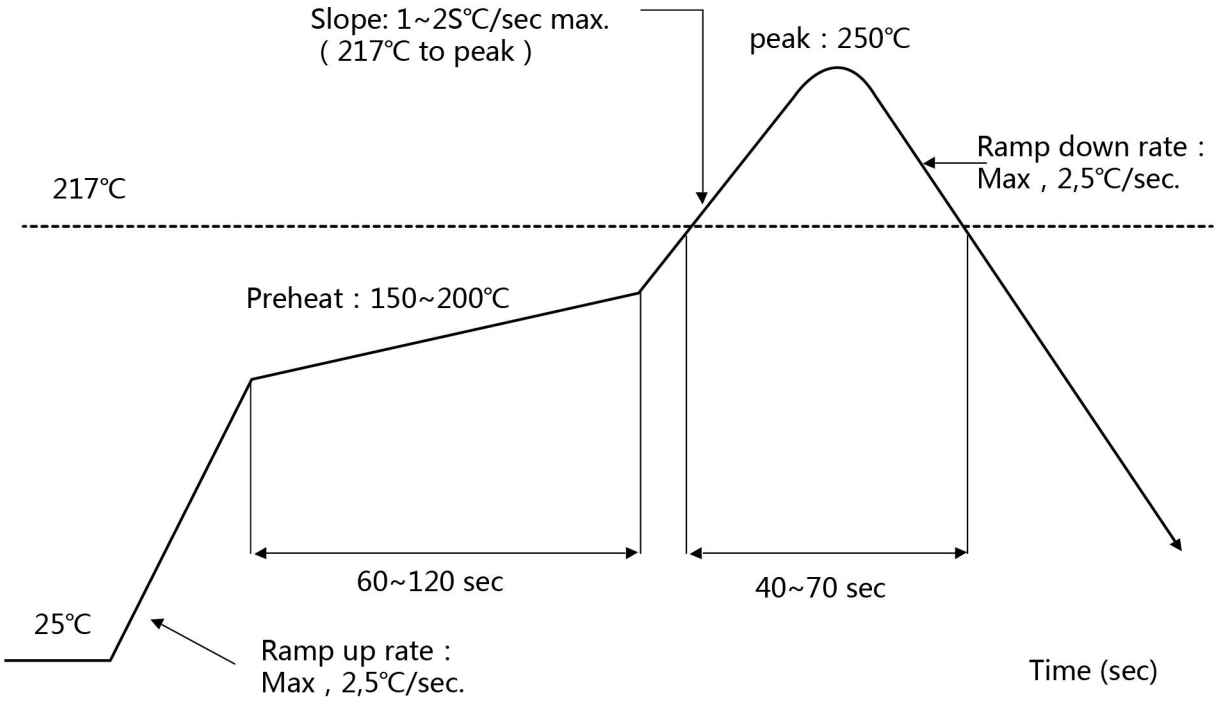


11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

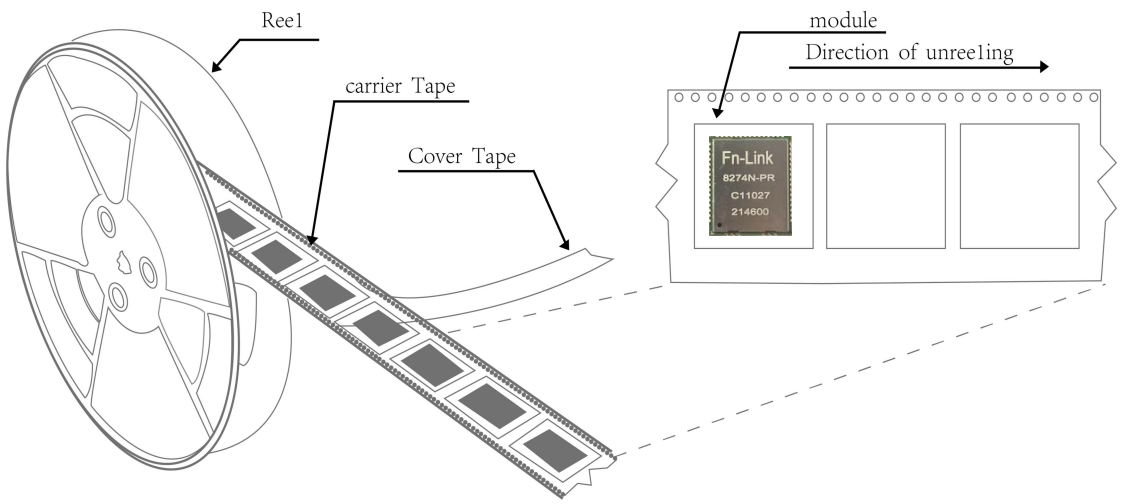
Number of Times : ≤2 times



12. Package

12.1 Reel

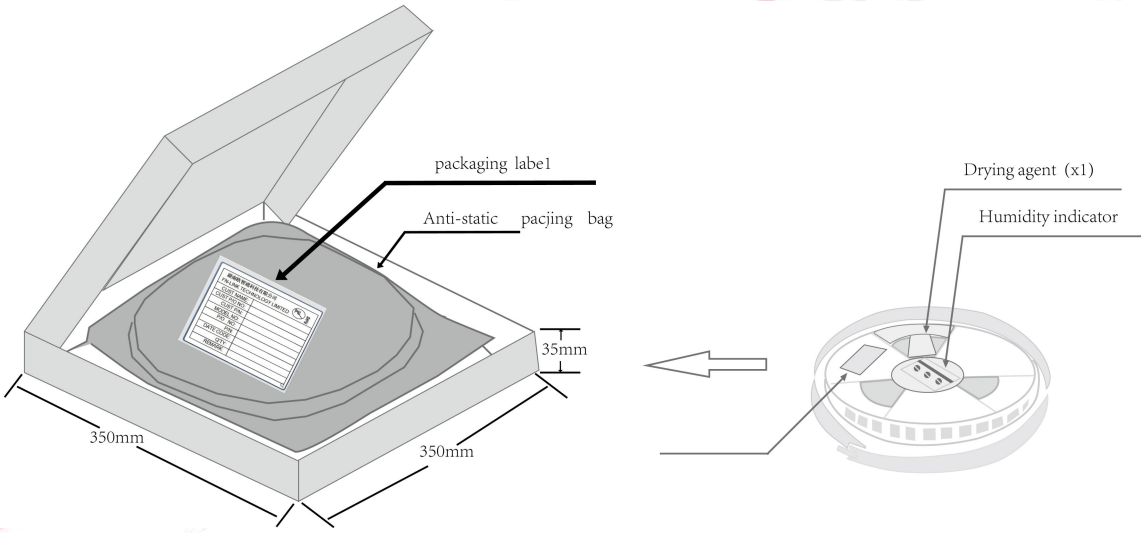
A roll of 1000pcs

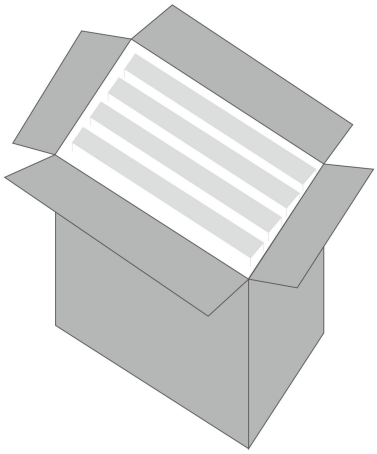


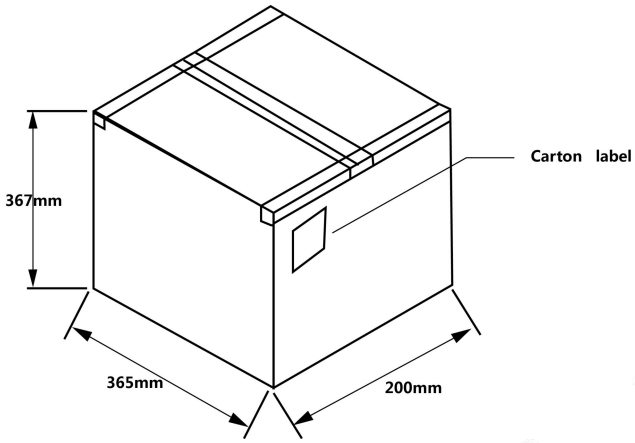
12.2 Carrier Tape Detail

NA

12.3 Packaging Detail







13. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more