

PRODUCT SPECIFICATION

6221B-SRC

Wi-Fi Dual-band 1x1 11b/g/n/ac + Bluetooth 4.2

Combo Module

Version:v1.4



6221B-SRC Module Datasheet

Ordering Information	Part NO.	Description
	FG6221BSRC-01	RTL8821CS,a/b/g/n/ac+BT4.2,1T1R,13*15,SDIO3.0/UART, 2 Antenna.WLAN pin9
	FG6221BSRC-L1	RTL8821CS,a/b/g/n/ac+BT4.2,1T1R,13*15,SDIO3.0 /UART,2 Antenna.WLAN pin9 (美磊双工器)

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

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1. General Description

1.1 Introduction

6221B-SRC support 1-stream 802.11ac solution with Mu-MIMO STA mode with Bluetooth smart ready controller, SDIO1.1/2.0/3.0 interface, HS-UART mixed interface. It combines WLAN MAC, a 1T1R WLAN baseband, RF in a single chip.

Module complies with IEEE 802.11 a/b/g/n/ac standard and the speed can achieve up to 433Mbps.

Module complies with bluetooth core specification V4.2. support dual mode (BR/EDR+low energy controllers). for low energy, it supports mutiple states and allows active links in master mode and don't support scatternet topology.

1.2 Description

Model Name	6221B-SRC
Product Description	Support Wi-Fi/Bluetooth functionalities
Dimension	L x W x H: 15 x 13 x 2.4 mm (typical)
Wi-Fi Interface	Support SDIO 1.1/2.0/3.0
BT Interface	UART / PCM
OS supported	Android /Linux/ Win CE /iOS /XP/WIN7/WIN10
Operating temperature	0° C to 70° C
Storage temperature	-40° C to 85° C

2. Features

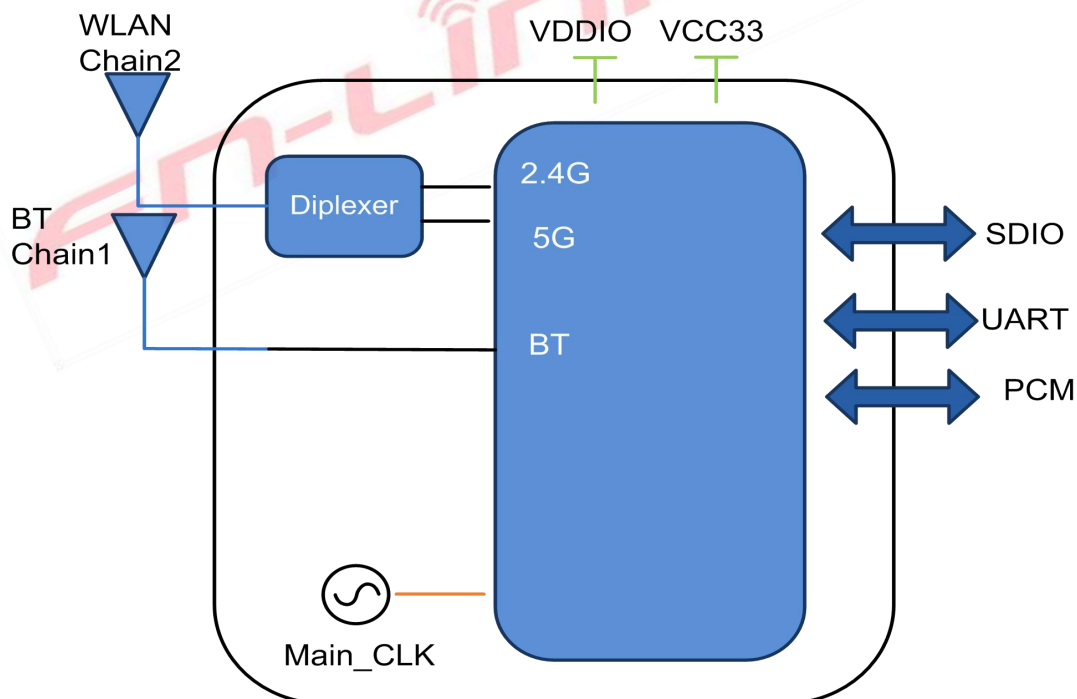
General Features

- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11 a/b/g/n/ac.
- Support 802.11ac 1x1, wave-2 compliant with MU-MIMO STA mode.
- SDIO 1.1/2.0/3.0 for WLAN with clock up to 100MHz.
- 802.11ac support maximum rate up to 433Mbps in 80MHz bandwidth.
- WLAN via pin9

Bluetooth Features

- HS-UART with configurable baud rate for BT.
- Supports Bluetooth V4.2 features.
- PCM interface for audio data.
- BT 4.0 dual mode support: simultaneous LE and BR/EDR.

3. Block Diagram



4. General Specification

4.1 2.4GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant	
Frequency Range	2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band)	
Number of Channels	2.4GHz: Ch1 ~ Ch14	
Test Items	Typical Value	EVM
Output Power	802.11b /11Mbps : 17dBm ± 2 dB	EVM ≤ -9dB
	802.11g /54Mbps : 15dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 14dBm ± 2 dB	EVM ≤ -28dB
Spectrum Mask	Meet with IEEE standard	
Freq. Tolerance	± 20ppm	
Test Items	TYP Test Value	Standard Value
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps PER @ -92 dBm	≤-83
	- 2Mbps PER @ -90 dBm	≤-80
	- 5.5Mbps PER @ -87 dBm	≤-79
	- 11Mbps PER @ -85 dBm	≤-76
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps PER @ -89 dBm	≤-85
	- 9Mbps PER @ -88 dBm	≤-84
	- 12Mbps PER @ -87 dBm	≤-82
	- 18Mbps PER @ -84 dBm	≤-80
	- 24Mbps PER @ -81 dBm	≤-77
	- 36Mbps PER @ -78 dBm	≤-73
	- 48Mbps PER @ -73 dBm	≤-69
- 54Mbps PER @ -71 dBm	≤-68	
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -89 dBm	≤-85
	- MCS=1 PER @ -86 dBm	≤-82
	- MCS=2 PER @ -84 dBm	≤-80
	- MCS=3 PER @ -80 dBm	≤-77
	- MCS=4 PER @ -77 dBm	≤-73
	- MCS=5 PER @ -72 dBm	≤-69
	- MCS=6 PER @ -71 dBm	≤-68
- MCS=7 PER @ -69 dBm	≤-67	
SISO Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0, PER @ -88 dBm	≤-82
	- MCS=1, PER @ -85 dBm	≤-79

	- MCS=2, PER @ -83 dBm	≤-77
	- MCS=3, PER @ -79 dBm	≤-74
	- MCS=4, PER @ -76 dBm	≤-70
	- MCS=5, PER @ -71 dBm	≤-66
	- MCS=6, PER @ -70 dBm	≤-65
	- MCS=7, PER @ -68 dBm	≤-64
Maximum Input Level	802.11b : -10 dBm	
	802.11g/n : -20 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

4.2 5GHz RF Specification

Feature	Description	
WLAN Standard	IEEE 802.11a/n/ac 1x1, Wi-Fi compliant	
Frequency Range	5.150 GHz ~ 5.850 GHz (5.0 GHz Band)	
Number of Channels	5.0GHz: Please see the table1	
Test Items	Typical Value	EVM
Output Power	802.11a /54Mbps : 13 dBm ± 2 dB	EVM ≤ -25dB
	802.11n /MCS7 : 12 dBm ± 2 dB	EVM ≤ -28dB
	802.11ac /MCS9 : 10 dBm ± 2 dB	EVM ≤ -32dB
Test Items	Test Value	Standard Value
Receive Sensitivity (11a, 20MHz) @10% PER	- 6Mbps PER @ -87 dBm	≤-82
	- 9Mbps PER @ -85 dBm	≤-81
	- 12Mbps PER @ -84 dBm	≤-79
	- 18Mbps PER @ -82 dBm	≤-77
	- 24Mbps PER @ -78 dBm	≤-74
	- 36Mbps PER @ -75 dBm	≤-70
	- 48Mbps PER @ -70 dBm	≤-66
	- 54Mbps PER @ -69 dBm	≤-65
Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -85 dBm	≤-82
	- MCS=1 PER @ -83 dBm	≤-79
	- MCS=2 PER @ -80 dBm	≤-77
	- MCS=3 PER @ -77 dBm	≤-74
	- MCS=4 PER @ -73 dBm	≤-70
	- MCS=5 PER @ -69 dBm	≤-66

	- MCS=6	PER @ -67 dBm	≤-65
	- MCS=7	PER @ -66 dBm	≤-64
Receive Sensitivity (11n,40MHz) @10% PER	- MCS=0	PER @ -82 dBm	≤-81
	- MCS=1	PER @ -79 dBm	≤-78
	- MCS=2	PER @ -78 dBm	≤-76
	- MCS=3	PER @ -73 dBm	≤-72
	- MCS=4	PER @ -70 dBm	≤-69
	- MCS=5	PER @ -65 dBm	≤-64
	- MCS=6	PER @ -64 dBm	≤-63
	- MCS=7	PER @ -62 dBm	≤-61
Receive Sensitivity (11ac,20MHz) @10% PER	- MCS=0	PER @ -86 dBm	≤-82
	- MCS=1	PER @ -84 dBm	≤-81
	- MCS=2	PER @ -81 dBm	≤-79
	- MCS=3	PER @ -78 dBm	≤-74
	- MCS=4	PER @ -74 dBm	≤-71
	- MCS=5	PER @ -70 dBm	≤-67
	- MCS=6	PER @ -68 dBm	≤-66
	- MCS=7	PER @ -67 dBm	≤-61
Receive Sensitivity (11ac,40MHz) @10% PER	- MCS=8	PER @ -63 dBm	≤-59
	- MCS=0	PER @ -82 dBm	≤-79
	- MCS=1	PER @ -78 dBm	≤-76
	- MCS=2	PER @ -76 dBm	≤-73
	- MCS=3	PER @ -73 dBm	≤-69
	- MCS=4	PER @ -70 dBm	≤-68
	- MCS=5	PER @ -65 dBm	≤-64
	- MCS=6	PER @ -63 dBm	≤-63
	- MCS=7	PER @ -61 dBm	≤-58
	- MCS=8	PER @ -59 dBm	≤-56
- MCS=9	PER @ -58 dBm	≤-54	
Receive Sensitivity (11ac,80MHz) @10% PER	- MCS=0	PER @ -78 dBm	≤-76
	- MCS=1	PER @ -75 dBm	≤-73
	- MCS=2	PER @ -73 dBm	≤-71
	- MCS=3	PER @ -69 dBm	≤-68
	- MCS=4	PER @ -66 dBm	≤-64
	- MCS=5	PER @ -64 dBm	≤-60
	- MCS=6	PER @ -60 dBm	≤-59
	- MCS=7	PER @ -58 dBm	≤-58

	- MCS=8 PER @ -55 dBm	≤-53
	- MCS=9 PER @ -54 dBm	≤-51
Maximum Input Level	802.11a/n : -30 dBm	
Antenna Reference	Small antennas with 0~2 dBi peak gain	

Conditions : VBAT=3.3V ; VDDIO=3.3V ; Temp:25°C

15GHz(20MHz) Channel table

Band range	Operating Channel Numbers	Channelcenter frequencies(MHz)
5180MHz~5240MHz	36	5180
	40	5200
	44	5220
	48	5240
5260MHz~5320MHz	52	5260
	56	5280
	60	5300
	64	5320
5550MHz~5700MHz	100	5500
	104	5520
	108	5540
	112	5560
	116	5580
	120	5600
	124	5620
	128	5640
	132	5660
	136	5680
	140	5700
5745MHz~5825MHz	149	5745
	153	5765
	157	5785
	161	5805
	165	5825

4.3 Bluetooth Specification

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V4.2		
Host Interface	UART		
Antenna Reference	Small antennas with 0~2 dBi peak gain		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	GFSK, $\pi/4$ -DQPSK, 8-DPSK		
RF Specification			
	Min(dBm)	Typical(dBm)	Max(dBm)
Output Power (Class 1)	0	5	10
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-92	
Sensitivity @ BER=0.01% for $\pi/4$ -DQPSK (2Mbps)		-86	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-85	
Maximum Input Level	GFSK (1Mbps):-20dBm		
	$\pi/4$ -DQPSK (2Mbps) :-20dBm		
	8DPSK (3Mbps) :-20dBm		

5. ID setting information

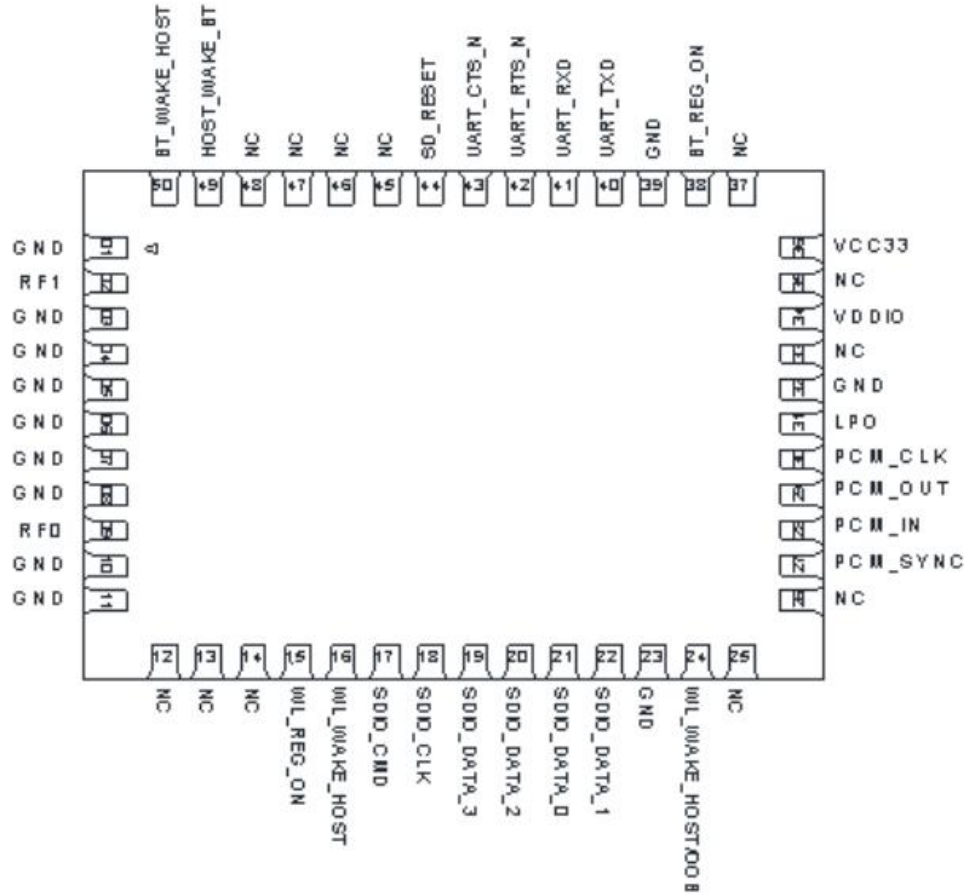
WI-FI

Vendor ID	-
Product ID	-

6. Pin Definition

6.1 Pin Outline

< TOP VIEW >



6.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND	—	Ground connections	
2	RF1	I/O	RF I/O port for BT	
3	GND	—	Ground connections	
4	GND	—	Ground connections	
5	GND	—	Ground connections	

6	GND	—	Ground connections	
7	GND	—	Ground connections	
8	GND	—	Ground connections	
9	RF0	I/O	RF I/O port for 2.4+5G	
10	GND	—	Ground connections	
11	GND	—	Ground connections	
12	NC	—	No connect	
13	NC	—	No connect	
14	NC	—	No connect	
15	WL_REG_ON	I	GPIO9, SD RESET This pin can externally shut down WLAN function when pulled low <i>该功能已不支持，关闭 wifi 请使用卸载驱动的方式</i>	VDDIO
16	WL_WAKE_HOST	O	GPIO10. WLAN to wake-up HOST	VDDIO
17	SDIO_CMD	I/O	SDIO command line	VDDIO
18	SDIO_CLK	I/O	SDIO clock line	VDDIO
19	SDIO_DATA_3	I/O	SDIO data line 3	VDDIO
20	SDIO_DATA_2	I/O	SDIO data line 2	VDDIO
21	SDIO_DATA_0	I/O	SDIO data line 0	VDDIO
22	SDIO_DATA_1	I/O	SDIO data line 1	VDDIO
23	GND	—	Ground connections	
24	WL_WAKE_HOST	O	GPIO10. Same function with pin16	VDDIO
25	NC	—	No connect	
26	NC	—	No connect	
27	PCM_SYNC	I/O	PCM sync signal	VDDIO
28	PCM_IN	I	PCM data input	VDDIO
29	PCM_OUT	O	PCM Data output	VDDIO
30	PCM_CLK	I/O	PCM clock	VDDIO
31	LPO	I	External Low Power Clock input (32.768KHz) If not used keep NC	
32	GND	—	Ground connections	
33	NC	—	No connect	
34	VDDIO	P	I/O Voltage supply input	1.8V or 3.3V
35	NC	—	No connect	
36	VCC33	P	Main power voltage source input	3.3V

37	NC	—	No connect	
38	BT_REG_ON	I	Enable pin for Bluetooth device Default ON: pull high ; OFF: pull low External pull low to shut down BT	VDDIO
39	GND	—	Ground connections	
40	UART_TXD	O	Bluetooth UART interface	VDDIO
41	UART_RXD	I	Bluetooth UART interface	VDDIO
42	UART_RTS_N	O	Bluetooth UART interface	VDDIO
43	UART_CTS_N	I	Bluetooth UART interface	VDDIO
44	SD RESET	—	GPIO9, SD RESET This pin can externally shut down WLAN function when pulled low。 Suggest NC this PIN.	
45	NC	—	No connect	
46	GND	—	Module ground connection.	
47	NC	—	No connect	
48	GND	—	Module ground connection.	
49	HOST_WAKE_BT	I	HOST wake-up Bluetooth device	VDDIO
50	BT_WAKE_HOST	O	Bluetooth device to wake-up HOST	VDDIO

P:POWER I:INPUT O:OUTPUT VDDIO:1.8V or 3.3V

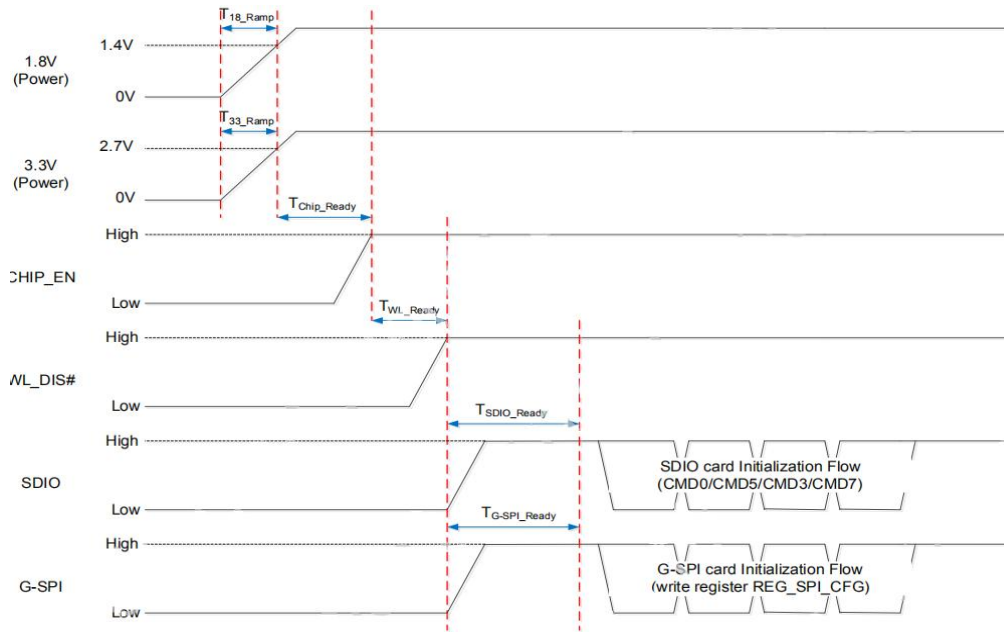
7. Electrical Specifications

7.1 Power Supply DC Characteristics

	MIN	TYP	MAX	Unit
Operating Temperature	0	25	70	deg.C
VCC33	3.15	3.3	3.45	V
VDDIO	1.7	1.8 or 3.3	3.45	V

7.2 Interface Circuit time series

7.2.1 system power on sequence



System Power-On Sequence

	Min	Typical	Max	Unit	Description
T _{18_Ramp}	0.1	0.5	2.5	ms	The 1.8V main power ramp up duration.
T _{33_Ramp}	0.1	0.5	2.5	ms	The 3.3V main power ramp up duration.
T _{Chip_Ready}					CHIP_EN pull high timing
T _{WL_Ready}				ms	WL_DIS# pull high timing
T _{SDIO_Ready}	1	2	10	ms	SDIO Not Ready Duration. In this state, the RTL8821CS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure.
T _{G-SPI_Ready}	3	4	18	ms	The duration G-SPI device internal initialization. After

7.2.2 SDIO Pin Description

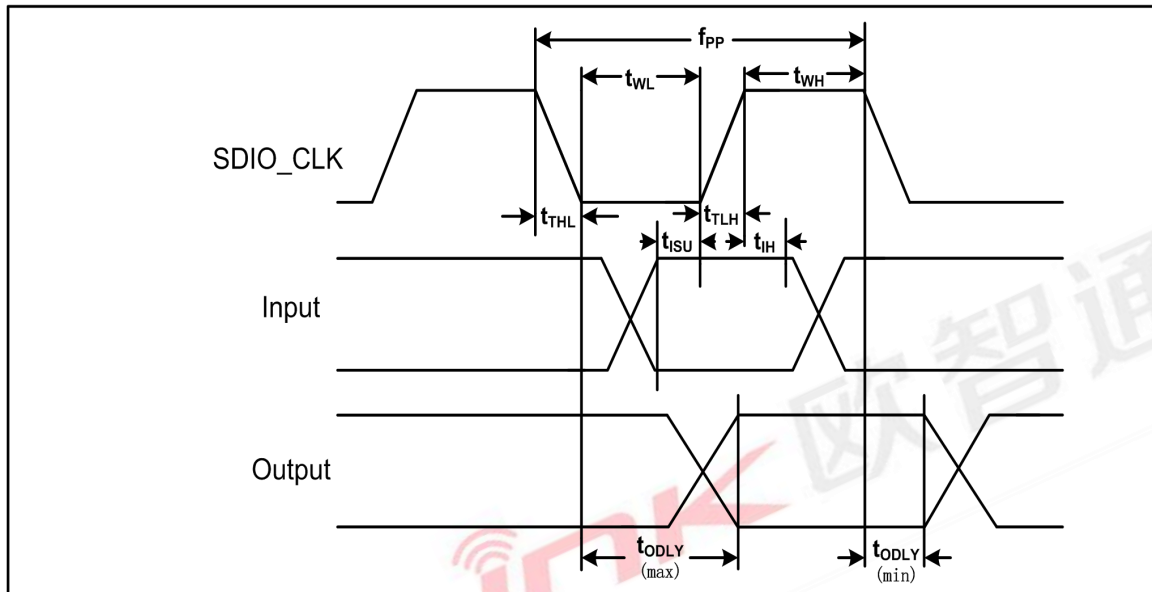
The module supports SDIO version 3.0 for all 1.8V to 3.3V.

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait

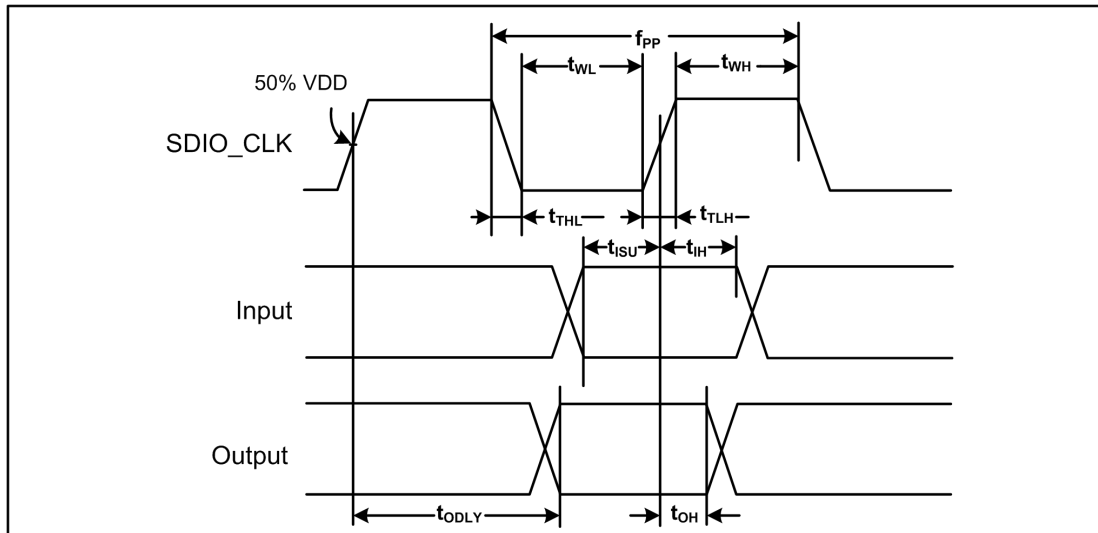
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

7.2.3 SDIO Default Mode Timing Diagram



Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK(All values are referred to minimum VIH and maximum VIL^b)					
Frequency - Data Transfer mode	fPP	0	-	25	MHz
Frequency - Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	10	-	-	ns
Clock high time	tWH	10	-	-	ns
Clock rise time	tTLH	-	-	10	ns
Clock low time	tTHL	-	-	10	ns
Inputs:CMD, DAT(referenced to CLK)					
Input setup time	tISU	5	-	-	ns
Input hold time	tIH	5	-	-	ns
Outputs:CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	tODLY	0	-	14	ns
Output delay time - Identification mode	tODLY	0	-	50	ns

- a. Timing is based on $CL \leq 40$ pF load on CMD and Data.
- b. $Min(V_{ih}) = 0.7 \times V_{DDIO}$ and $max(V_{il}) = 0.2 \times V_{DDIO}$.



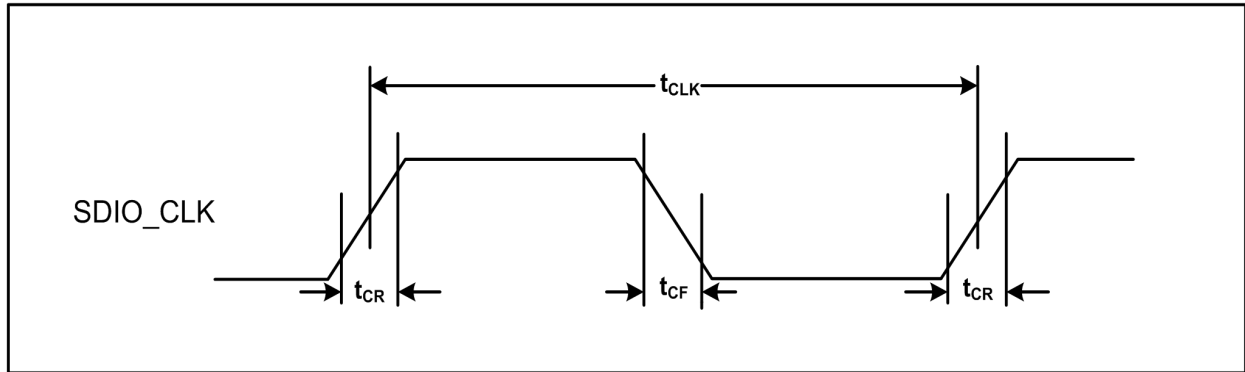
7.2.4 SDIO High Speed Mode Timing Diagram

Parameter	Symbol	Minimum	Typical	Maximum	Unit
SDIO CLK(all values are referred to minimum VIH and maximum VIL^b)					
Frequency - Data Transfer mode	fPP	0	-	50	MHz
Frequency - Identification mode	fOD	0	-	400	kHz
Clock low time	tWL	7	-	-	ns
Clock high time	tWH	7	-	-	ns
Clock rise time	tTLH	-	-	3	ns
Clock low time	tTHL	-	-	3	ns
Inputs:CMD, DAT(referenced to CLK)					
Input setup time	tISU	6	-	-	ns
Input hold time	tIH	2	-	-	ns
Outputs:CMD, DAT(referenced to CLK)					
Output delay time - Data Transfer mode	tODLY	-	-	14	ns
Output delay time - Identification mode	tODLY	2.5	-	-	ns
Total system capacitance(each line)	CL	-	-	40	pF

- Timing is based on $CL \leq 40$ pF load on CMD and Data.
- $Min(V_{ih}) = 0.7 \times V_{DDIO}$ and $max(V_{il}) = 0.2 \times V_{DDIO}$.

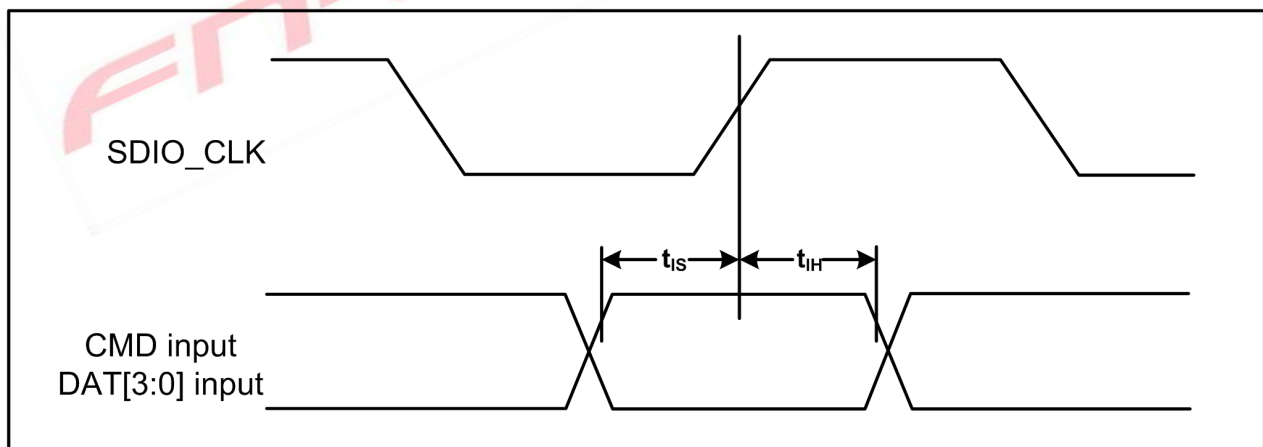
7.2.5 SDIO Bus Timing Specifications in SDR Modes

Clock timing(SDR Modes)



Parameter	Symbol	Minimum	Maximum	Unit	Comments
-	t_{CLK}	40	-	ns	SDR12 mode
-		20	-	ns	SDR25 mode
-		10	-	ns	SDR50 mode
-		4.8	-	ns	SDR104 mode
-	t_{CR}, t_{CF}	-	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 2.00$ ns (max)@100 MHz, $C_{CARD} = 10$ pF $t_{CR}, t_{CF} < 0.96$ ns (max)@208 MHz, $C_{CARD} = 10$ pF
Clock duty	-	30	70	%	-

Card Input timing (SDR Modes)



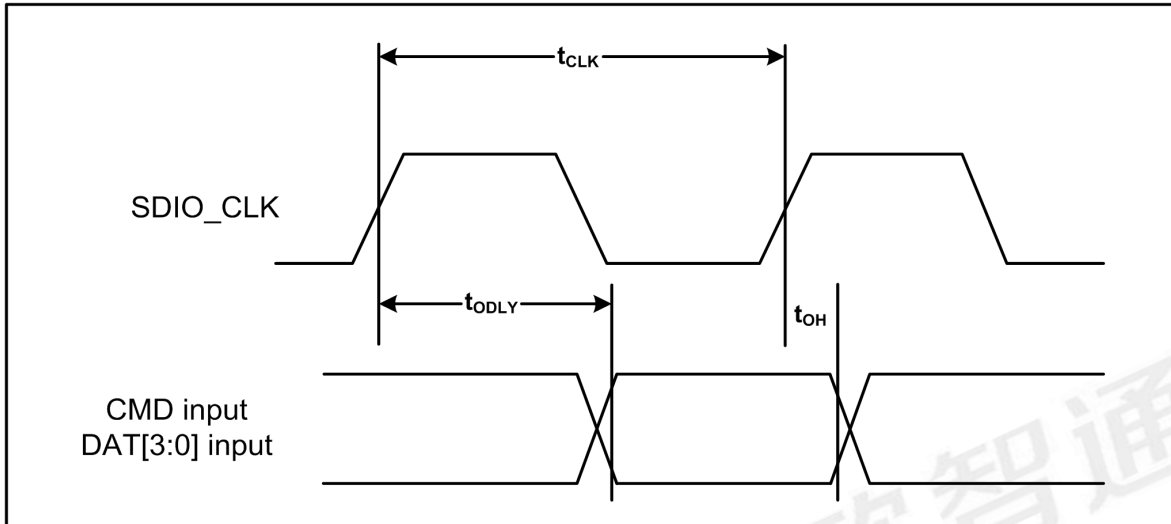
Symbol	Minimum	Maximum	Unit	Comments
SDR104 Mode				
t_{IS}	1.70 ^a	-	ns	$C_{CARD} = 10$ pF, VCT = 0.975V
t_{IH}	0.80	-	ns	$C_{CARD} = 5$ pF, VCT = 0.975V

SDR50 Mode

t_{IS}	3.00	-	ns	$C_{CARD} = 10pF, V_{CT} = 0.975V$
t_{IH}	0.80	-	ns	$C_{CARD} = 5pF, V_{CT} = 0.975V$

a. SDIO 3.0 specification value is 1.40 ns

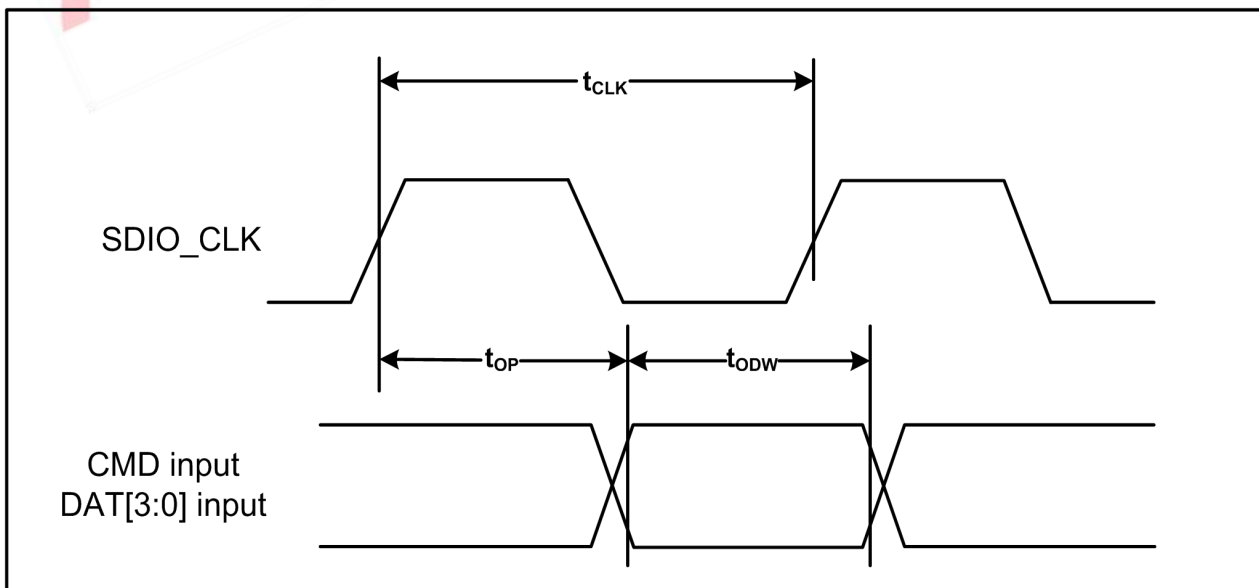
Card output timing (SDR Modes up to 100MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{ODLY}	-	7.85 ^a	ns	$t_{CLK} \geq 10$ ns $C_L = 30$ pF using driver type B for SDR50
t_{ODLY}	-	14.0	ns	$t_{CLK} \geq 20$ ns $C_L = 40$ pF using for SDR12, SDR25
t_{OH}	1.5	-	ns	Hold time at the $t_{ODLY}(\min)$ $C_L = 15$ pF

a. SDIO 3.0 specification value is 7.5 ns.

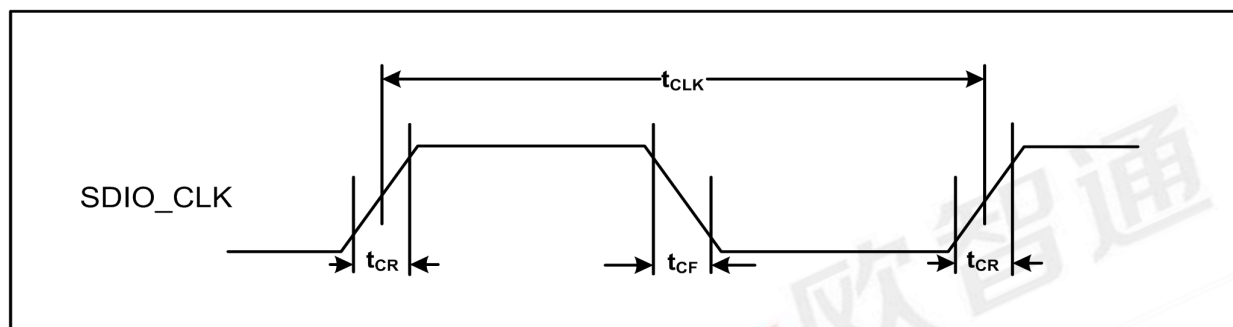
Card output timing (SDR Modes 100MHz to 208MHz)



Symbol	Minimum	Maximum	Unit	Comments
t_{OP}	0	2	UI	Card output phase
Δt_{OP}	-350	+1550	ps	Delay variation due to temp change after tuning
t_{ODW}	0.6	-	UI	$t_{ODW} = 2.88 \text{ ns @ } 208 \text{ MHz}$

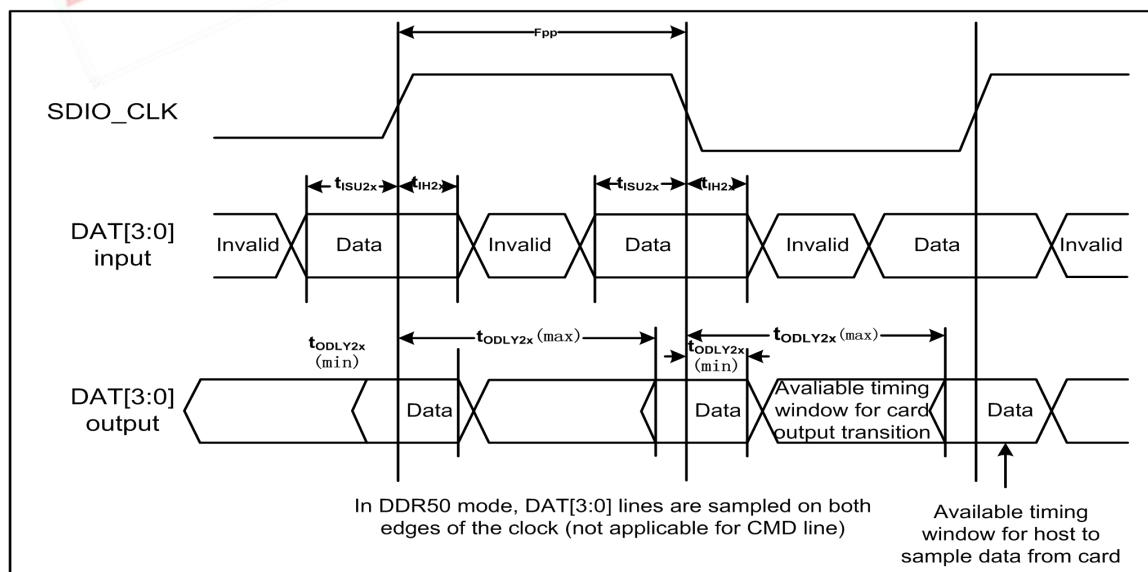
- $\Delta t_{OP} = +1550 \text{ ps}$ for junction temperature of $\Delta t_{OP} = 90$ degrees during operation
- $\Delta t_{OP} = -350 \text{ ps}$ for junction temperature of $\Delta t_{OP} = -20$ degrees during operation
- $\Delta t_{OP} = +2600 \text{ ps}$ for junction temperature of $\Delta t_{OP} = -20$ to $+125$ degrees during operation

7.2.6 SDIO Bus Timing Specifications in DDR50 Mode



parameter	Symbol	Minimum	Maximum	Unit	Comments
-	t_{CLK}	20	-	ns	DDR50 mode
-	t_{CR}, t_C	-	$0.2 \times t_{CLK}$	ns	$t_{CR}, t_{CF} < 4.00 \text{ ns (max) @ } 50 \text{ MHz, } C_{CARD} = 10 \text{ pF}$
Clock duty	-	45	55	%	-

Data Timing



In DDR50 mode, DAT[3:0] lines are sampled on both edges of the clock (not applicable for CMD line)


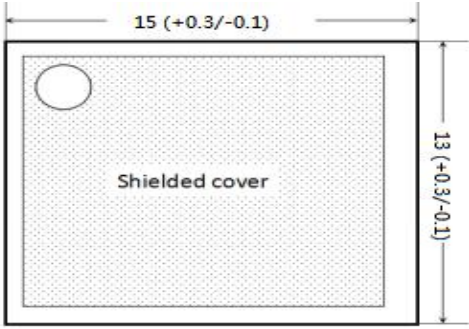
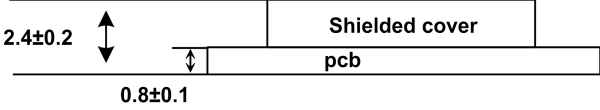
Available timing window for host to sample data from card

parameter	Symbol	Minimum	Maximum	Unit	Comments
Input CMD					
Input setup time	t _{ISU}	6	-	ns	C _{CARD} < 10 pF (1 Card)
Input hold time	t _{IH}	0.8	-	ns	C _{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t _{ODLY}	-	13.7	ns	C _{CARD} < 30 pF (1 Card)
Output hold time	t _{OH}	1.5	-	ns	C _{CARD} < 15 pF (1 Card)
Input DAT					
Input setup time	t _{ISU2x}	3	-	ns	C _{CARD} < 10 pF (1 Card)
Input hold time	t _{IH2x}	0.8	-	ns	C _{CARD} < 10 pF (1 Card)
Output CMD					
Output delay time	t _{ODLY2x}	-	7.85 ^a	ns	C _{CARD} < 25 pF (1 Card)
Output hold time	t _{ODLY2x}	1.5	-	ns	C _{CARD} < 15 pF (1 Card)

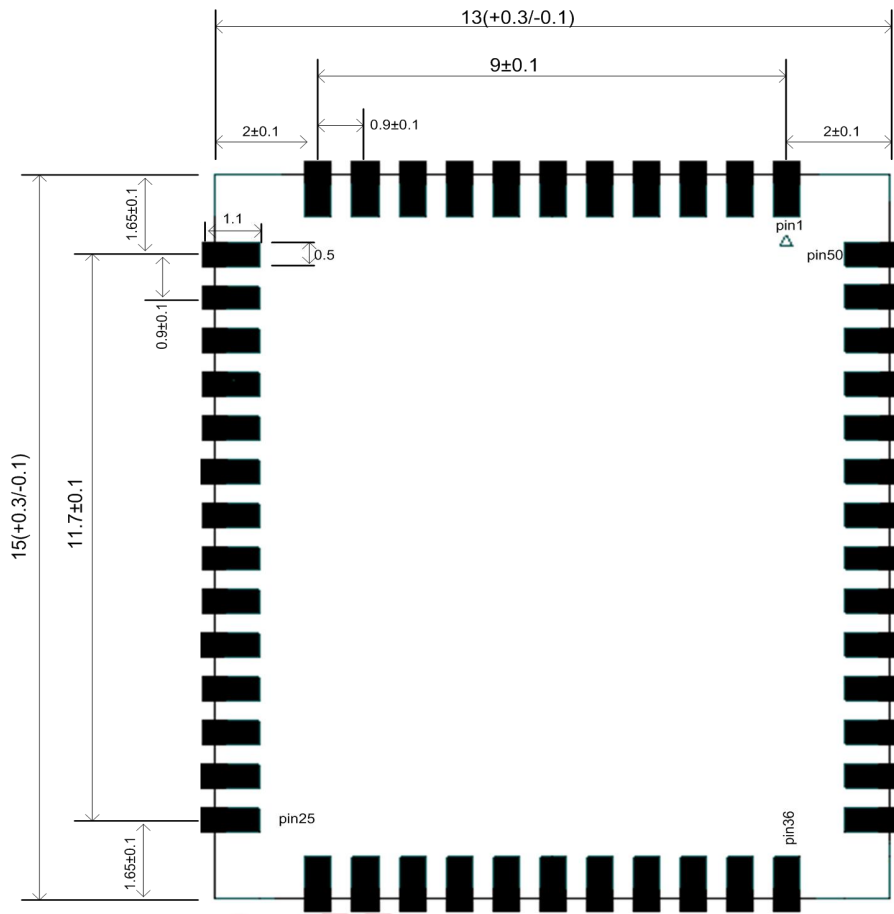
a. SDIO 3.0 specification value is 7.0 ns

8. Size reference

8.1 Module Picture

<p>L x W : 15 x 13 (+0.3/-0.1) mm</p> 	
<p>H: 2.4 (±0.2) mm</p>	
<p>Weight</p>	<p>0.6g</p>

8.4 Layout Recommendation

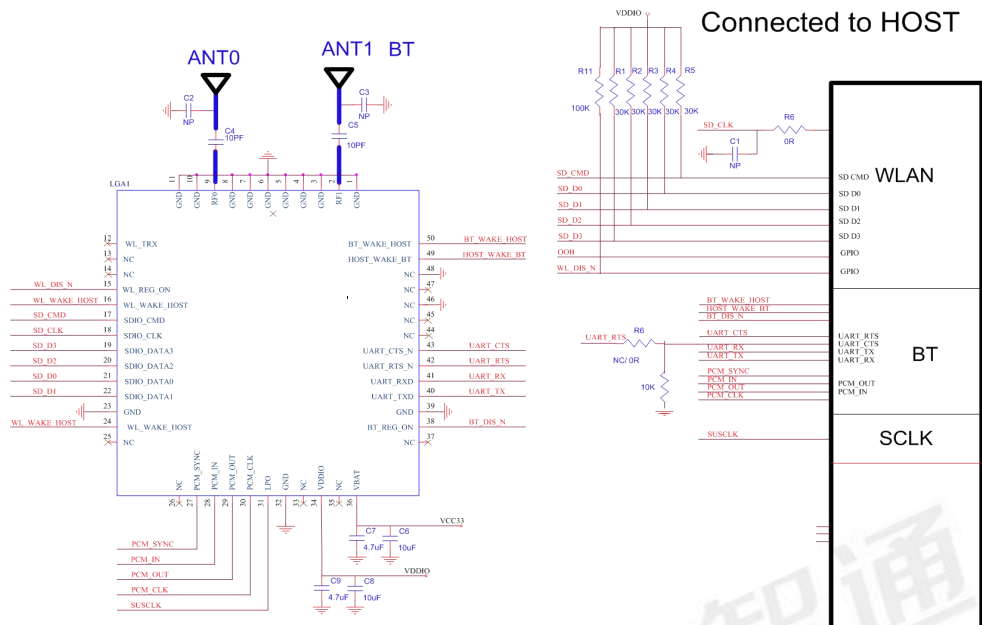


9. The Key Material List

Item	Part Name	Description	Manufacturer
1	PCB	6221B-SRC,green,FR4,Au,13*15-0.8mm	Sunlord,xy-pcb,kx-pcb,sl-pcb
2	Crystal	2520 40MHz 10ppm 12PF	ECEC,TKD,Hosonic,JWT
3	Chipset	RTL8821CS BGA	Realtek
4	Shielding	6221B-SRC Shielding	信太, 精力通
5	TVS	0201 4V 0.05pF 15KV TVS	Murata,Sunlord,Way-on
6	Diplexer	DP1608-2.4GGHz+5GHz	ACX,walsin,Glead,Maglayers
7	Inductor	0806 2.2uH, ± 20%,1200mA	Sunlord,ceaiya,cenke,Microgate

10. Reference Design

50 ohm RF trace



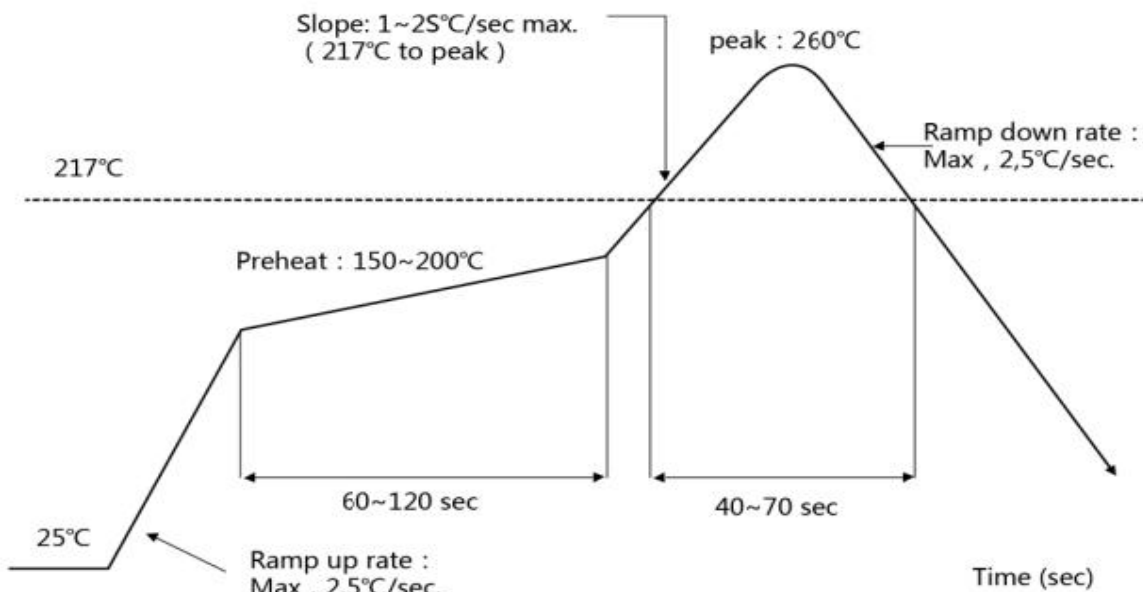
C6, C7 caps should be closed to pin36 of the module
C8, C9 caps should be closed to pin34 of the module

11. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260°C

Number of Times : ≤2 times



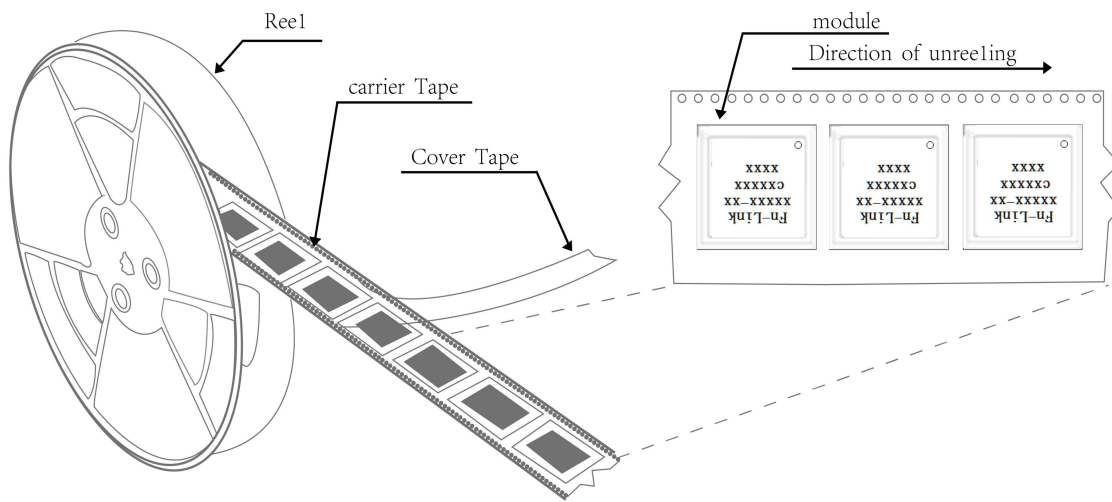
12. RoHS compliance

All hardware components are fully compliant with EU RoHS directive

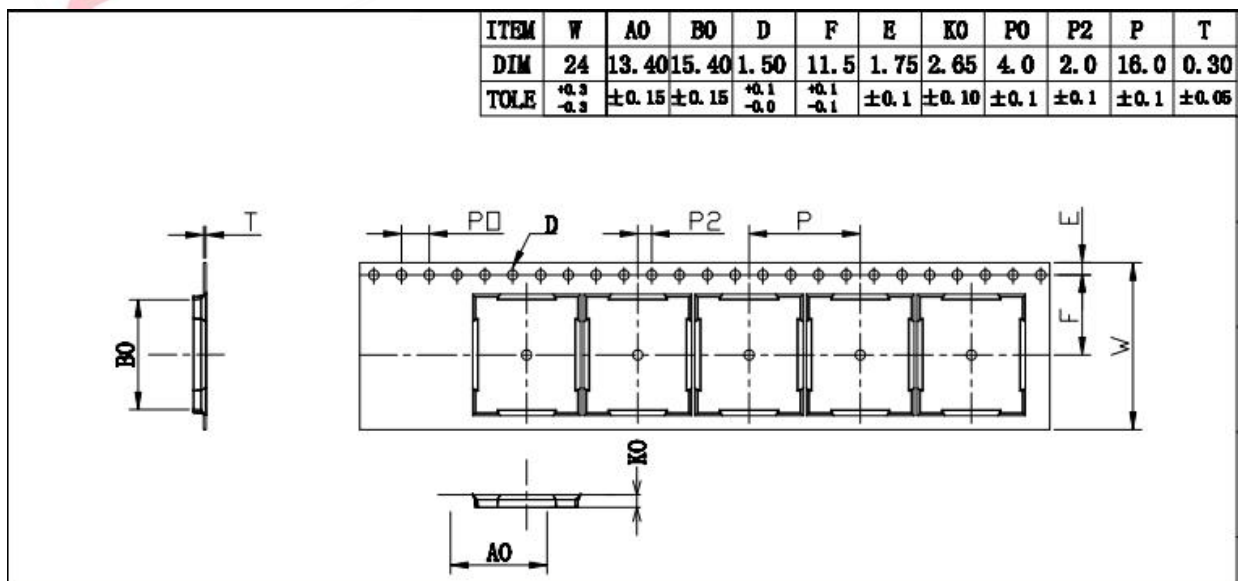
13. Package

13.1 Reel

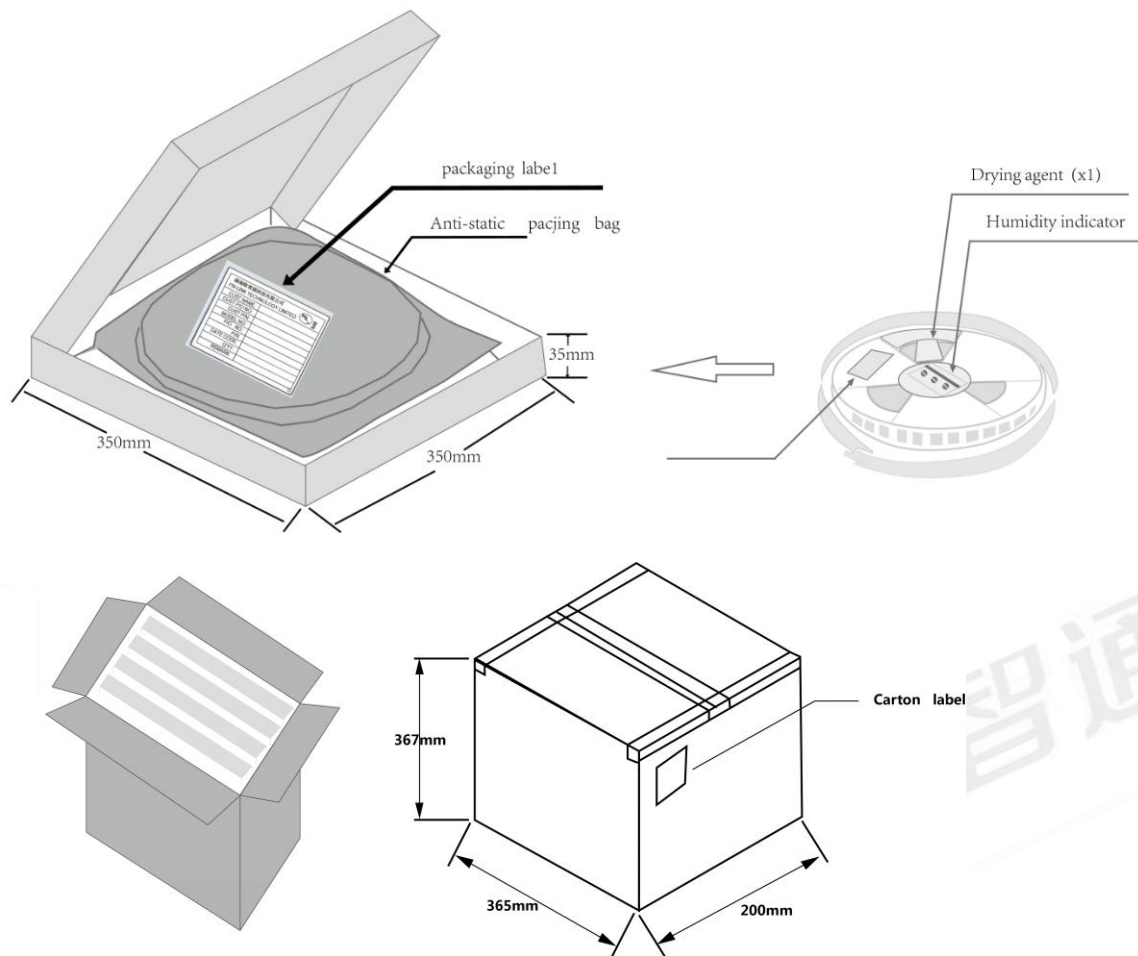
A roll of 1500pcs



13.2 Carrier Tape Detail



13.3 Packaging Detail



14. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

- Calculated shelf life in sealed bag: 12 months at <math><40^{\circ}\text{C}</math> and <math><90\%</math> relative humidity (RH)
- Environmental condition during the production: - The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
- “IPC/JEDEC J-STD-033A paragraph 5.2” is respected
- Baking is required if conditions b) or c) are not respected
- Baking is required if the humidity indicator inside the bag indicates 10% RH or more