PRODUCT SPECIFICATION

4108N-S

IEEE 802.11ah Wireless LAN

Module Datasheet

Version:v1.0

Customer: _____

Customer P/N: _____

Signature: _____

Date: _____

Office: 14th floor, Block B, phoenix zhigu, Xixiang Street, Baoan District, Shenzhen

Factory: NO.8, Litong RD., Liuyang Economic & Technical Development Zone, Changsha, CHINA

TEL: +86-755-2955-8186 Website: www.fn-link.com

4108N-S Module Datasheet

	Part NO.	Description
Ordering Information	FG4108NSXX-00	MM6108,802.11ah,1G,WIFI,1T1R,23X14mm,SDIO+SPI

CONTENTS

Revision History

Version	Date	Contents of Revision Change	Draft	Checked	Approved
V1.0	2023/08/28	New version	Lxp	Sxl	Qjp

1. General Description

1.1 Introduction

Fnlink introduces the pioneer of the IEEE 802.11ah WIFI LGA module --- 4108N-S. The 4108N-S is an IEEE 802.11ah Wi-Fi module designed in compliance with the IEEE 802.11ah standard, supporting data rates up to 32Mbps that operates in the Sub 1GHz license-exempt band, offering longer ranger and higher data rate for internet of things (IoT) applications. The 4108N-S enables streamlined data transfer interoperability with existing Wi-Fi networks while meeting up to 1Km long range data transfer with low power consumption requirements.

The 4108N-S integrated IEEE 802.11ah Sub-1G 8MHz Single-chip MAC/PHY/Radio SoC Morse Micro MM6108, ultra-long-reach PA, high linearity LNA, T/R switch, 32 MHz crystal and it has been designed for a simplified Wi-Fi HaLow connection to an external host for applications in which a customer wants to merely replace their prior RF technology with a Wi-Fi HaLow connection while leveraging the latest WPA3 security protocol. 4108N-S supports SDIO 2.0 compliant slave interface and SPI mode operation, and many peripherals such as general I2C, UART and GPIOs. In addition, its MAC supports for STA and AP roles.

1.2 Description

Model Name	4108N-S
Product Description	IEEE 802.11ah Wireless LAN Module
Major Chipset	Morse Micro MM6108 (48-pin QFN)
Form Factor	LGA module, 44 pins
Dimension	L x W x H: 23 x 14 x 2.4mm
Host Interface	SDIO/SPI
Antenna	For Stamp Module, “1T1R, external” ANT Main：TX/RX
Operating temperature	-40°C to 85°C
Storage temperature	-40°C to 85°C

2. Features

General

- Support 850 ~ 950MHz frequency band
- Support single-stream data rate up to 32.5Mbps @8MHz or 15 Mbps @4MHz channel.
- Support channel width options of 1/2/4 MHz
- Support Modulation and Coding Scheme (MCS) levels MCS 0-7 and MCS 10
- Modulation: BPSK & QPSK, 16-QAM & 64 -QAM
- Support for 1 MHz and 2 MHz duplicate modes

Host Interface

- SDIO 2.0 (slave) Default Speed (DS) at 25MHz
- SDIO 2.0 (slave) High Speed (HS) at 50MHz
- Support for both 1-bit and 4-bit data mode
- Support for SPI mode operation

Standards Supported

- IEEE Std 802.11ah-2016 compliant

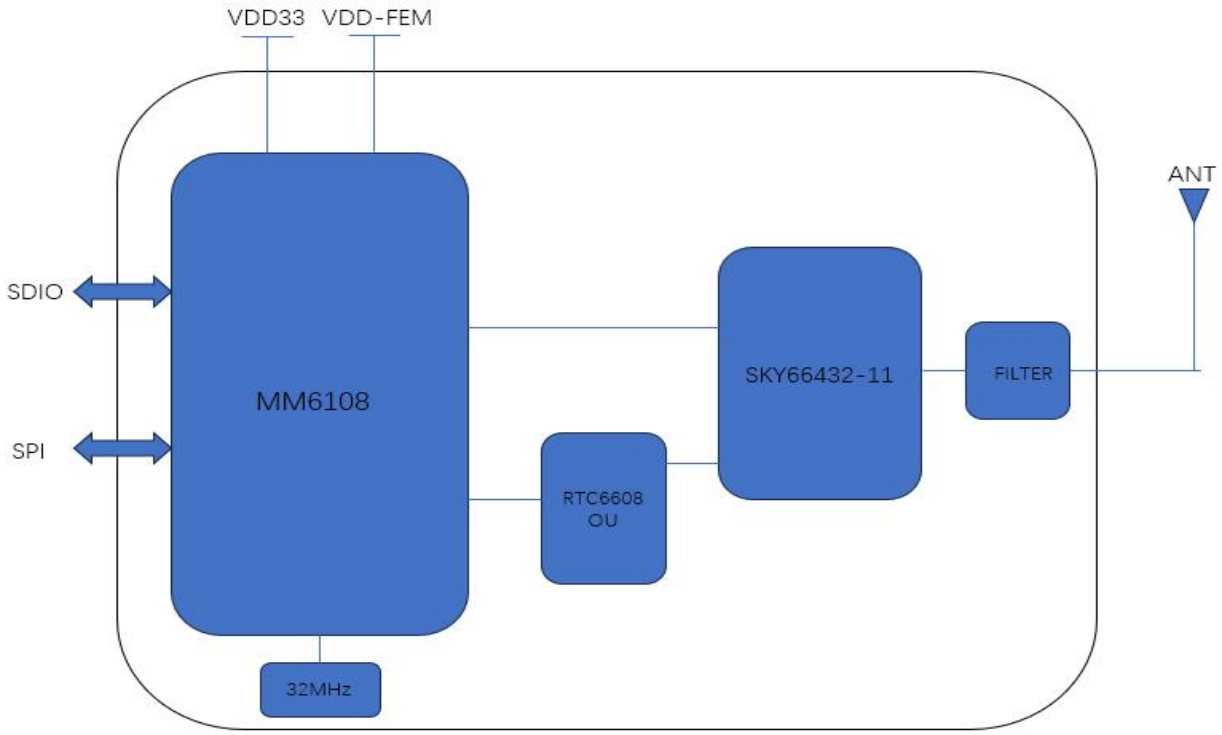
Security Features

- AES encryption engine
- Hardware support for SHA1 and SHA2 hash functions (SHA-256, SHA-384, SHA-512)
- WPA3 including protected management frames (PMF)
- Opportunistic Wireless Encryption (OWE)

Peripheral Interfaces

- SDIO/SPI, I2C and UART
- Support for STA and AP roles

3. Block Diagram



4. General Specification

4.1 WLAN Specification

Feature	**Description**	
WLAN Standard	IEEE 802.11ah	
Frequency Range	Japan 850 – 950 MHz	
Channel Bandwidth	1/2/4 MHz	
Modulation	BPSK, QPSK, 16-QAM, 64-QAM	
Test Items	**Typical Value**	
Output Power	MCS0 (1/2/4 MHz) : 16dbm	
	MCS7 (1/2/4MHz) : 12dbm	
	MCS10 (1 MHz) : 16dbm	
Receive Sensitivity	- MCS0 (1 MHz)	-105
	- MCS0 (2 MHz)	-103
	- MCS0 (4 MHz)	-101
	- MCS0 (8 MHz)	/

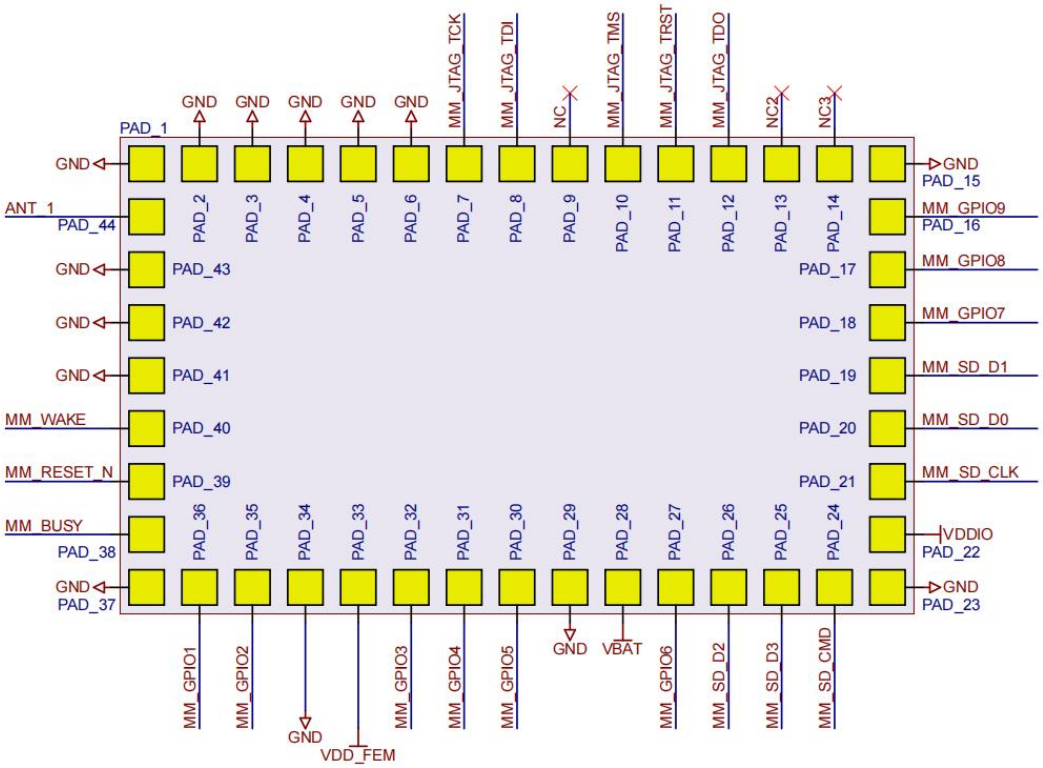
	- MCS7 (1 MHz)	-87
	- MCS7 (2 MHz)	-84
	- MCS7 (4 MHz)	-81
	- MCS7 (8 MHz)	/
	- MCS10 (1 MHz)	-107
Data Rate	1 MHz Bandwidth: up to 3.333Mbps 2 MHz Bandwidth: up to 7.222Mbps 4 MHz Bandwidth: up to 15Mbps	
Security	■ AES encryption engine ■ Hardware support for SHA1 and SHA2 hash functions (SHA-256,SHA-384,SHA-512) ■ WPA3 including protected management frames (PMF) ■ Opportunistic Wireless Encryption (OWE)	

* If you have any certification questions about output power please contact FAE directly.

5. Pin Definition

5.1 Pin Outline

< TOP VIEW >



5.2 Pin Definition details

NO.	Name	Type	Description	Voltage
1	GND		Ground connections	
2	GND		Ground connections	
3	GND		Ground connections	
4	GND		Ground connections	
5	GND		Ground connections	
6	GND		Ground connections	
7	MM_JTAG_TCK	I	JTAG clock	
8	MM_JTAG_TDI	I	JTAG data input	
9	NC		No Connection	
10	MM_JTAG_TMS	I	JTAG mode selection	
11	MM_JTAG_TRST	I	JTAG reset	
12	MM_JTAG_TDO	O	JTAG data output	
13	NC		No Connection	
14	NC		No Connection	
15	GND		Ground connections	
16	MM_GPIO9	I/O	General purpose I/O	VDDIO
17	MM_GPIO8	I/O	General purpose I/O	VDDIO
18	MM_GPIO7	I/O	General purpose I/O	VDDIO
19	MM_SD_D1	I/O	SDIO Data pin 1	
20	MM_SD_D0	I/O	SDIO Data pin 0	
21	MM_SD_CLK	I	SDIO Clock pin (input)	
22	VDDIO	P	I/O Voltage supply input 1.8V or 3.3V	1.8V/3.3V
23	GND		Ground connections	
24	MM_SD_CMD	I/O	SDIO Command pin	
25	MM_SD_D3	I/O	SDIO Data pin 3	
26	MM_SD_D2	I/O	SDIO Data pin 2	
27	MM_GPIO6	I/O	General purpose I/O	
28	VBAT	P	3.3V power supply	3.3V
29	GND		Ground connections	
30	MM_GPIO5	I/O	General purpose I/O	VDDIO
31	MM_GPIO4	I/O	General purpose I/O	VDDIO
32	MM_GPIO3	I/O	General purpose I/O	VDDIO
33	VDD_FEM	P	3.3V power supply for FEM	3.3V
34	GND		Ground connections	
35	MM_GPIO2	I/O	General purpose I/O	VDDIO

36	MM_GPIO1	I/O	General purpose I/O	VDDIO
37	GND		Ground connections	
38	MM_BUSY	I/O	General purpose I/O	VDDIO
39	MM_RESET_N	I/O	Reset (active low)	VDDIO
40	MM_WAKE	I	WAKE from sleep	
41	GND		Ground connections	
42	GND		Ground connections	
43	GND		Ground connections	
44	ANT	I/O	RF IN/OUT	

P:POWER I:INPUT O:OUTPUT VDDIO:1.8V/3.3V

6. Electrical Specifications

6.1 Power Supply DC Characteristics

	MIN	TYP	MAX	Unit
Operating Temperature	-40	25	85	deg.C
VBAT	3.0	3.3	3.6	V
VDDIO	1.8	3.3	VBAT	V

6.2 Power Consumption

Band (MHz)	Modulation	BW (MHz)	DUT Condition	VBAT = 3.3V VBAT (mA) AVG.
924	MCS0	1	Tx @ 16 dBm	185
		2		183
		4		187
		/		/
	MCS7	1	Tx @12 dBm	145
		2		148
		4		148
		/		/
	MCS10	1	Tx @ 16 dBm	195
Band	**Modulation**	**BW**	**DUT Condition**	**VBAT = 3.3V VBAT (mA)**

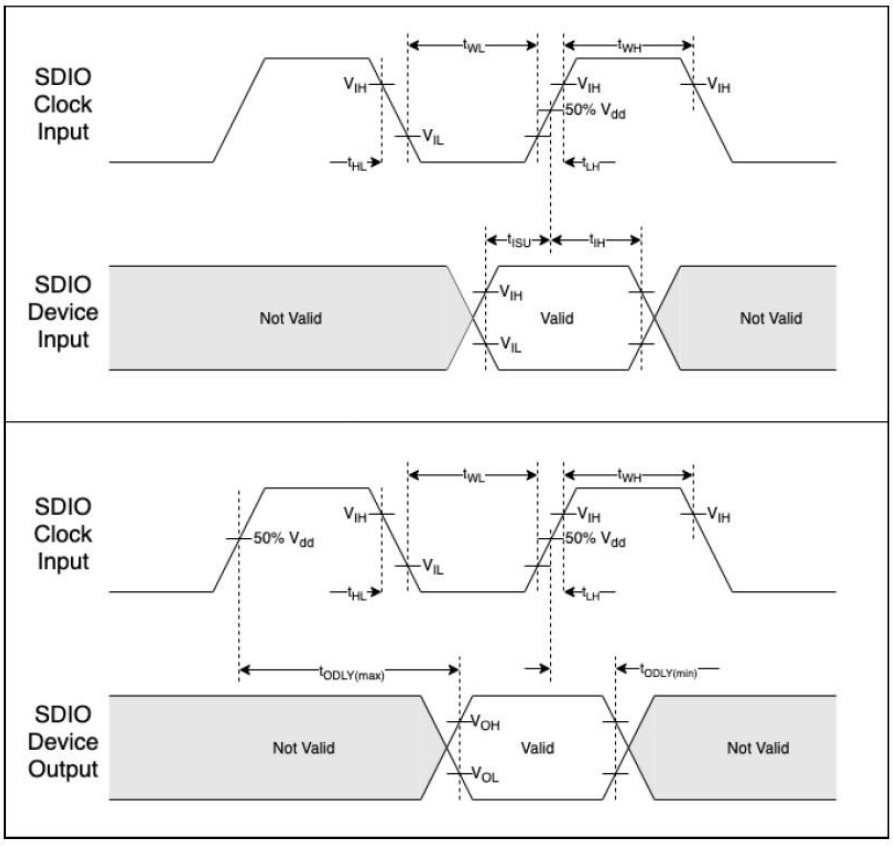
				Avg.
924	MCS0	1	Continuous Rx @ -105 dBm	31
		2	Continuous Rx @-103dBm	33
		4	Continuous Rx @ -101 dBm	41
		/	/	53
	MCS7	1	Continuous Rx @ -87 dBm	31
		2	Continuous Rx @ -84 dBm	35
		4	Continuous Rx @-81 -8dBm	45
		/	/	58
	MCS10	1	Continuous Rx @ -107 dBm	40

The power consumption is based on Fnlink test environment, these data for reference only.

6.3 Interface Circuit time series

6.3.1 SDIO Bus Timing

The SDIO clock rate supports up to 50MHz. The device always operates in SD high speed mode.



Parameter	Min	Max
Clock parameters		
Clock frequency	0MHz	50MHz
Clock low time (t_{WL})	7ns	
Clock high time(t_{WH})	7ns	
Clock rise time (t_{LH})		3ns
Clock fall time (t_{HL})		3ns
Inputs on CMD, DAT lines to device from host		
Input setup time (t_{ISU})	6ns	
Input hold time (t_{IH})	2ns	
Outputs on CMD, DAT lines from device to host		
Output delay ($t_{ODLY(max)}$)		14ns
Output hold time ($t_{ODLY(min)}$)	2.5ns	
Total system capacitance for each line		40pF

6.3.2 SPI Bus

The SPI clock rate supports up to 50MHz. The SPI bus timing is identical to the SDIO bus timing, where MOSI and MISO are considered input and output timing, respectively, in the SDIO timing specification.

The SPI bus defaults to clock idling at logical 0 (CPOL=0), and data is launched and captured on the positive edges of the clock, as per SDIO high-speed mode. It may be configured to behave like CPHA=0 (drive output on negative edge, sample on positive edge) after being initialized.

6.3.3 UART Bus

Two universal asynchronous receiver/transmitter (UARTs) are available and provide a means for serial communication to off-chip devices. The UART cores are as-provided by the SiFive IP repository. The UART peripheral does not support hardware flow control or other modem control signals, or synchronous serial data transfers.

We will clock the UARTs with a maximum clock speed of 30MHz (TBD), meaning maximum baud of the UART will be around 30Mbaud or 30Mbits/s if a divisor of 0 is specified.

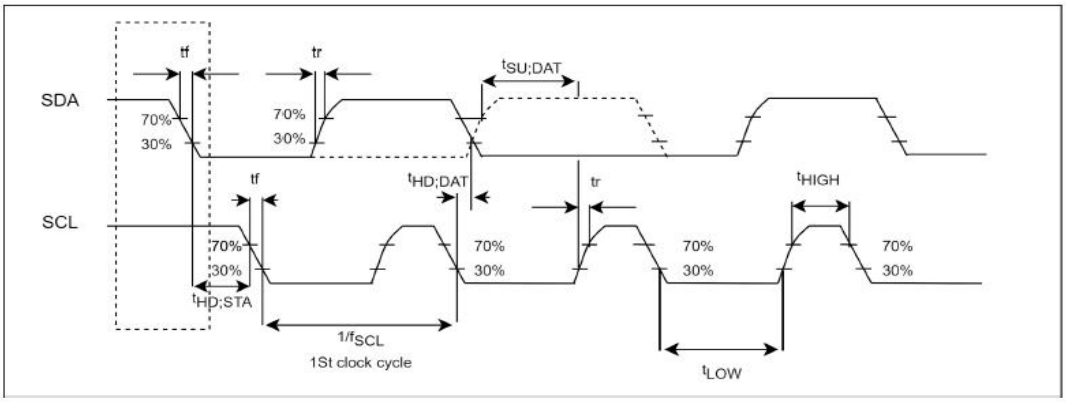
Pin	Name	Default Function	I/O Function
32	MM_GPIO7	GPIO	UART1 Tx
25	MM_GPIO6	GPIO	UART1 Rx
28	MM_GPIO3	GPIO	UART0 Tx
29	MM_GPIO2	GPIO	UART0 Rx

6.3.4 I2C Bus Timing

An I2C master interface is available. It consists of two lines, SDA and SCL, which are bidirectional, connected to a positive supply voltage via a current-source or pull-up resistor.

Pin	Name	Default Function	I/O Function
27	MM_GPIO4	GPIO	I2C SDA
26	MM_GPIO5	GPIO	I2C SCL

Definition of timing for F/S-mode devices on the I2C-bus. All values referred to



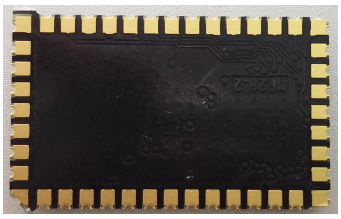
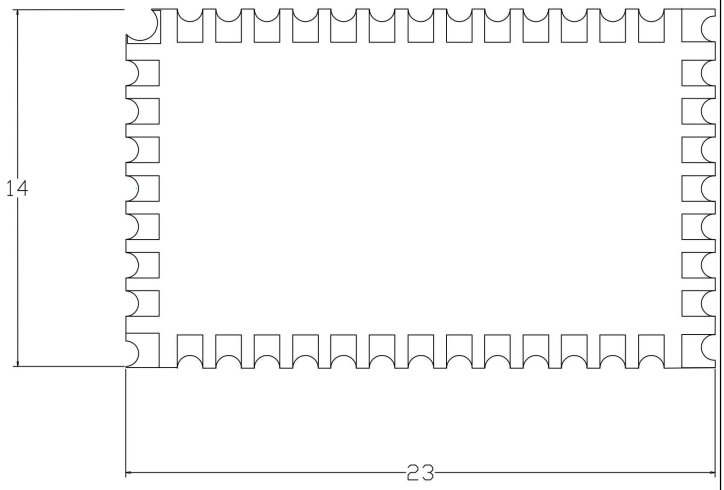
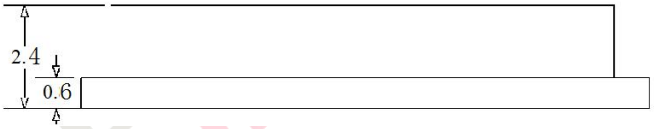
$V_{IH(min)}(0.3V_{DD})$ and $V_{IL(max)}(0.7V_{DD})$levels.

Parameter	Standard-mode		Fast-mode	
	Min	Max	Min	Max
Clock frequency(f_{SCL})	0	100kHz	0	400kHz
Fall time of both SDA and SCL (t_f)	-	300ns	20x (V_{DD}/5.5V)	300ns
Rise time of both SDA and SCL signals(t_r)	-	1000ns	20ns	300ns
Data hold time ($t_{HD;DAT}$)	5.0us	-	-	-
Data set-up time ($t_{SU;DAT}$)	250ns	-	100ns	-
LOW period of the SCL clock	4.7us	-	1.3us	-
HIGH period of the SCL clock	4.0us	-	0.6us	-
Hold time- START,first clock is generated after this($t_{HD;STA}$)	4us	-	0.6us	-

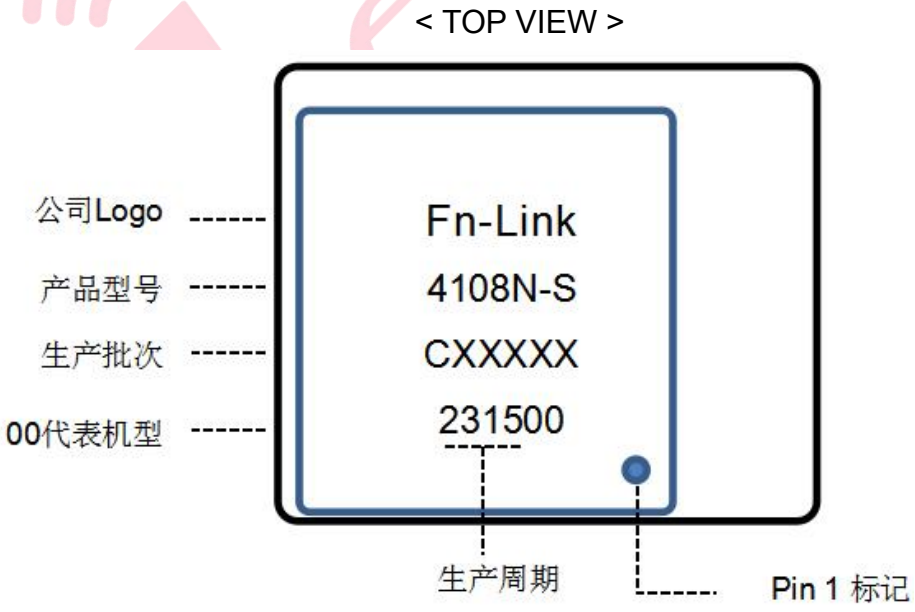
7. Size reference

7.1 Module Picture

<table>
<tr><td>L x W : 23 x 14 (±0.2) mm
 

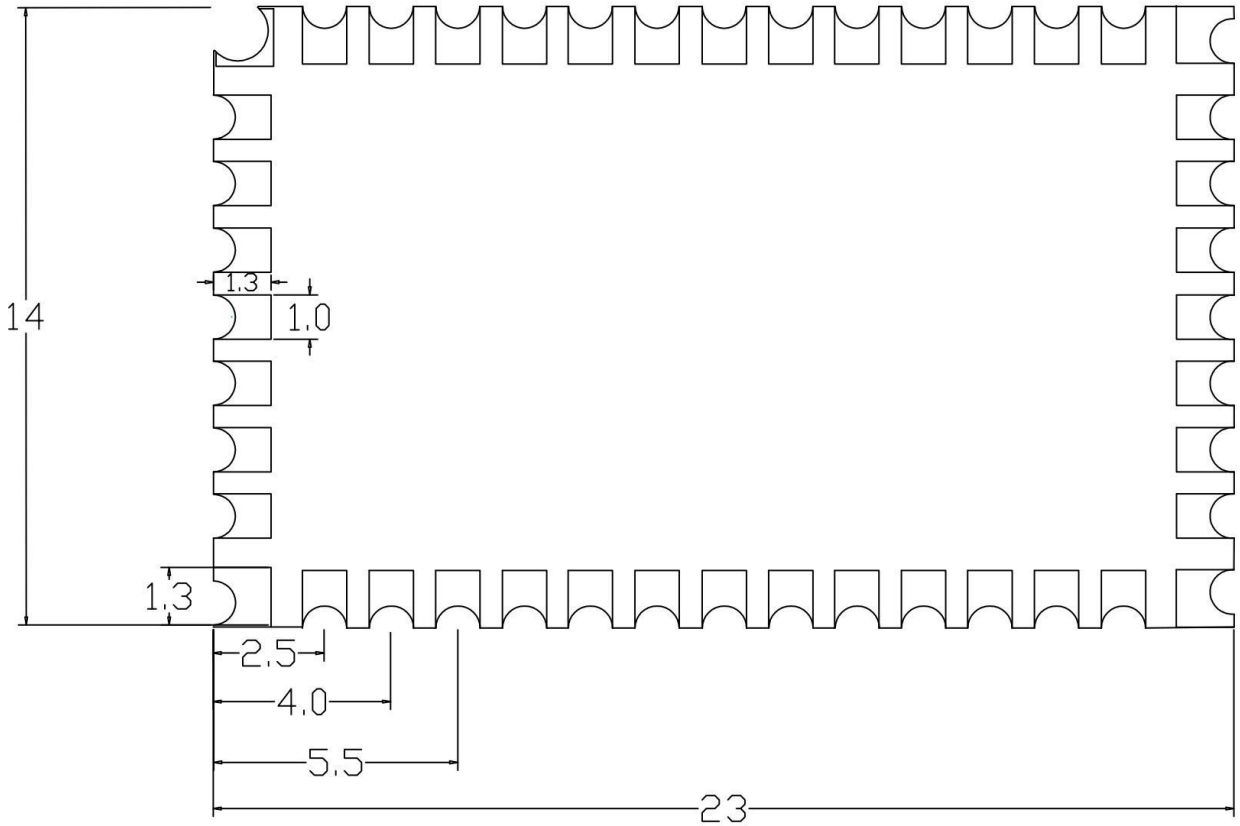
  </td><td> 
</td></tr>
<tr><td>H: 2.4 (±0.2) mm</td><td> 
</td></tr>
<tr><td>Weight</td><td>1.32g</td></tr>
</table>

7.2 Marking Description

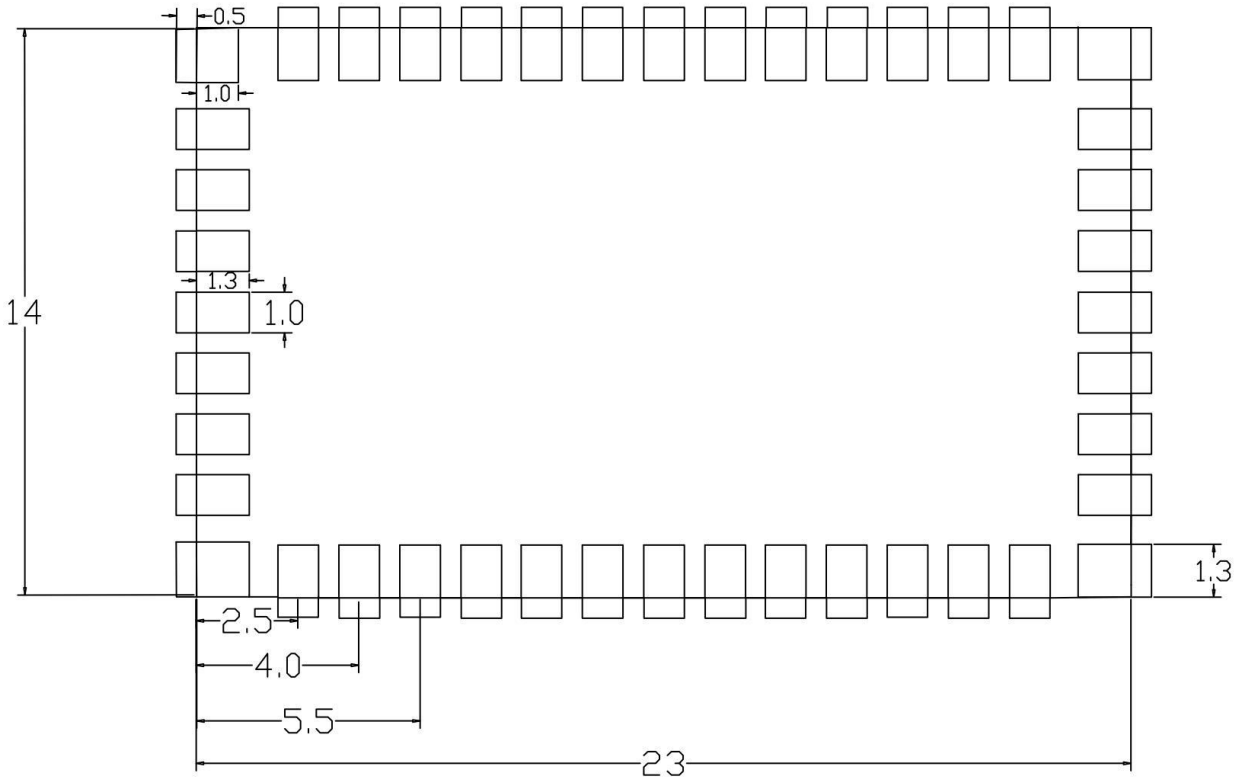


7.2 Physical Dimensions

<TOP View>



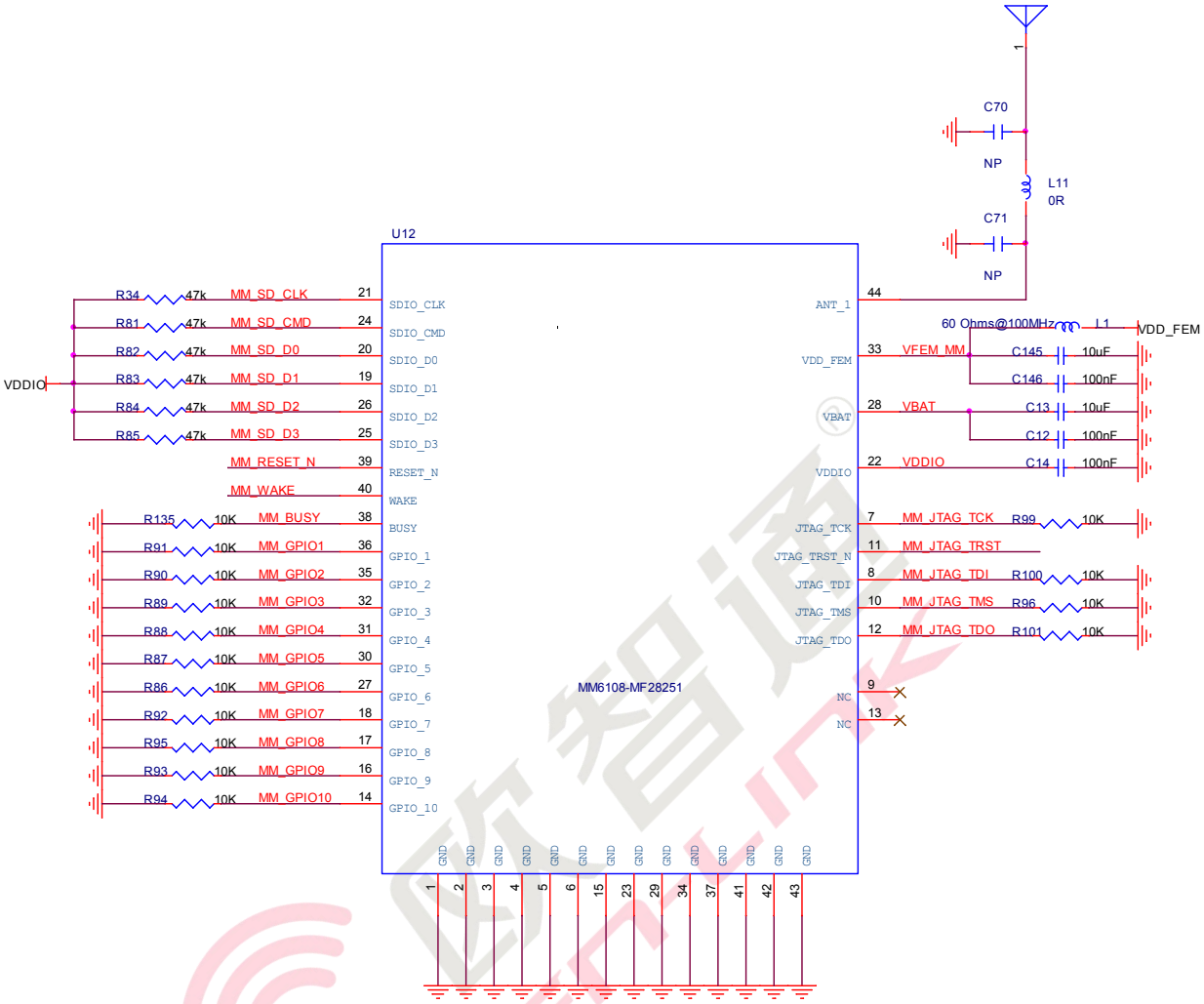
7.2 Layout Recommendation



8.The Key Material List

Item	Part Name	Description	Manufacturer
1	Crystal	1612 32MHZ,8PF,±10PPM,-30-85℃	Cenker,Sunlord, Ceaiya
2	Chipset	MM6108IQ-T,IEEE 802.11ah Sub-1 GHz 1/2/4/8MHz Bandwidth MAC/PHY/Radio SoC,QFN48	Morse Micro
3	PCB	4108N-S-V1.0 亮黑色,4 层板,FR4,TG150,无卤,金厚 2μ”,25 连片 23X14X0.6mm	XY-PCB,GDKX, Sunlord, SLPCB
4	Shielding	4108N-S-V1.0 屏蔽盖 21.64*12.84*1.7mm T=0.2mm,洋白铜,无定位脚	信太，精力通,卓益
5	FILTER	915MHZ 5SMD B39921B2625P810	Qualcomm
6	FEM	SKY66423-11,860 to 930MHz,2.0-4.8V,+27dbm,MCM 16pin	Skyworks
7	switch	RTC6608OU, 0.1-6.0GHz, 0.5dB insertion loss at 2GHz,QFN6	Richwave

9. Reference Design

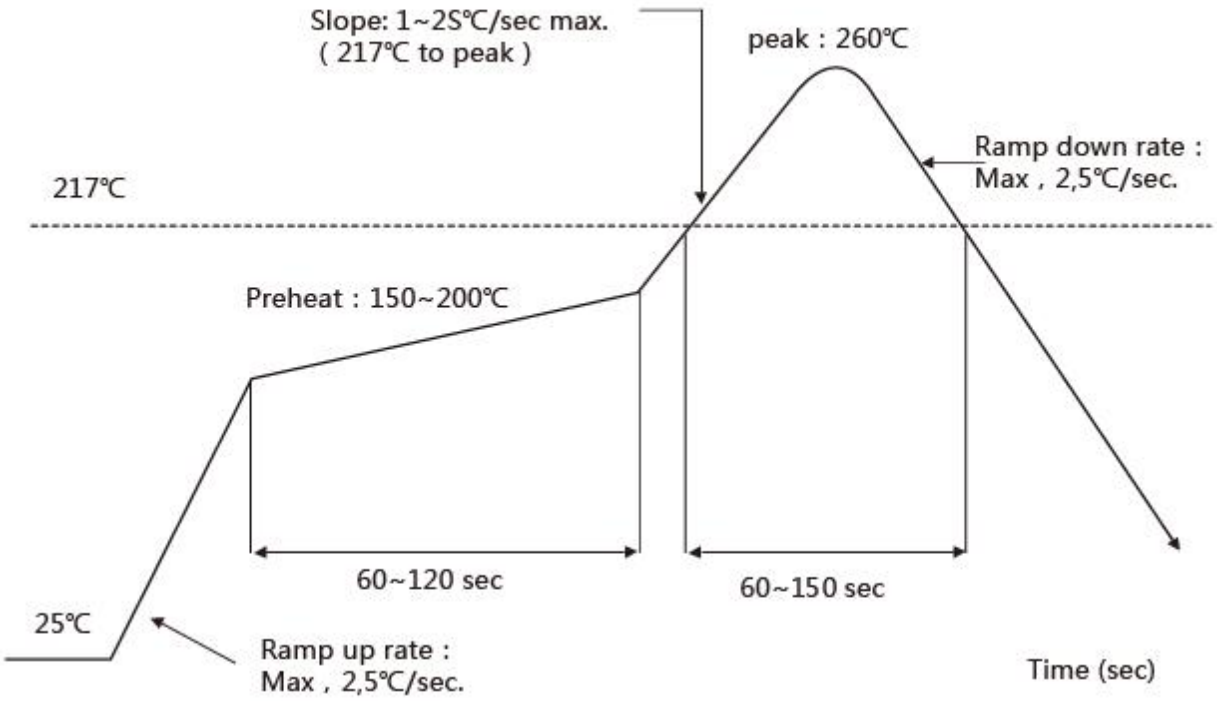


10. Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <260°C

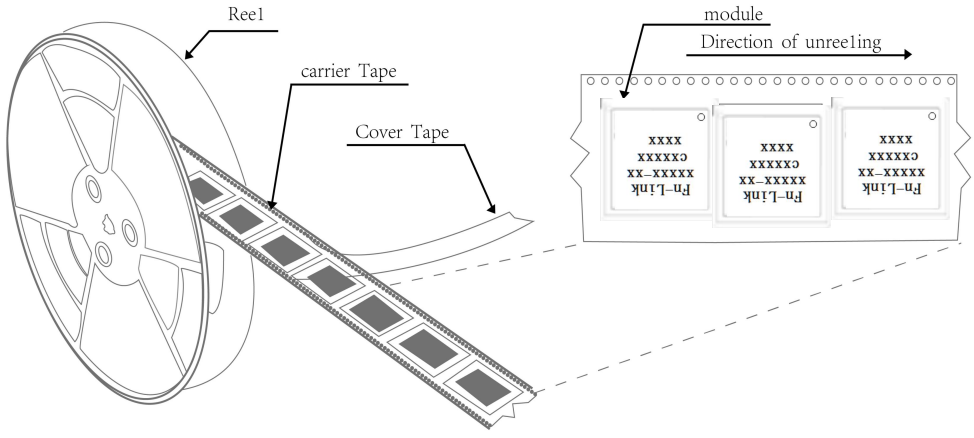
Number of Times : ≤2 times



11. Package

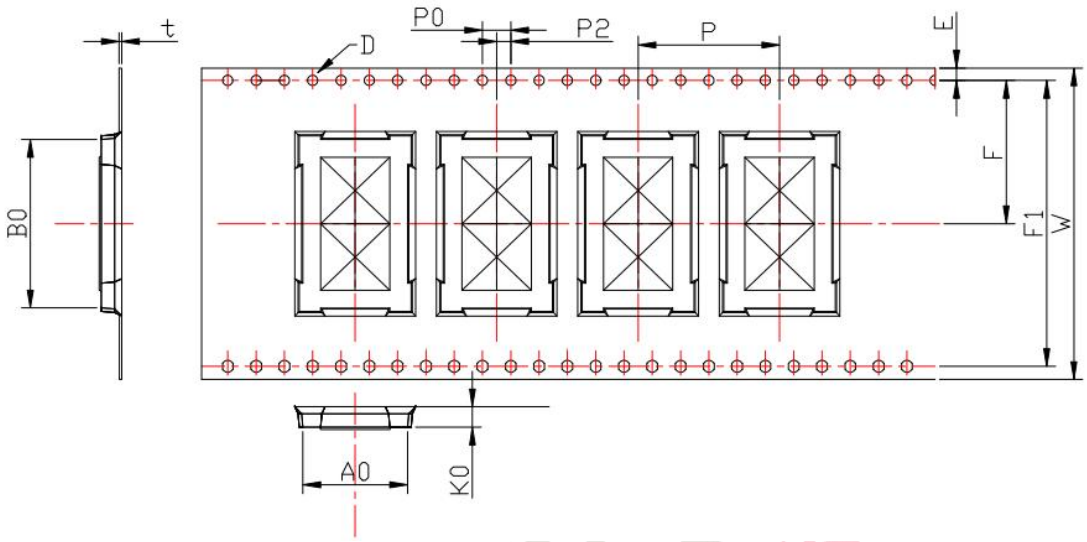
11.1 Reel

A roll of 1040pcs



11.2 Carrier Tape Detail

ITEM	W	A0	B0	D	E	F	F1	K0	P0	P2	P	T
DIM	44	14.45	23.45	1.5	1.75	20.2	40.4	2.90	4.0	2.0	20.0	0.30
TOLE	+0.3 -0.3	±0.15	±0.15	+0.1 -0.0	±0.1	±0.15	±0.10	±0.10	±0.1	±0.15	±0.1	±0.05



11.3 Packaging Detail

the take-up package

Using self-adhesive tape

Size of black tape: 24mm*32.6m the cover tape :21.3mm*32.6m

Color of plastic disc: blue

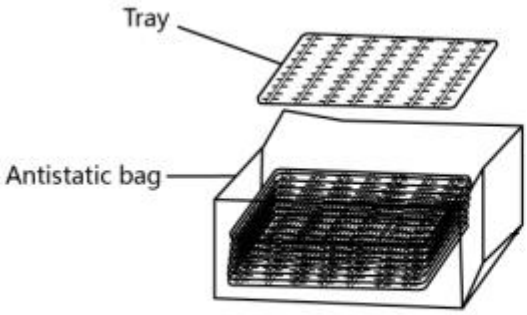
NY bag size:460mm*385mm

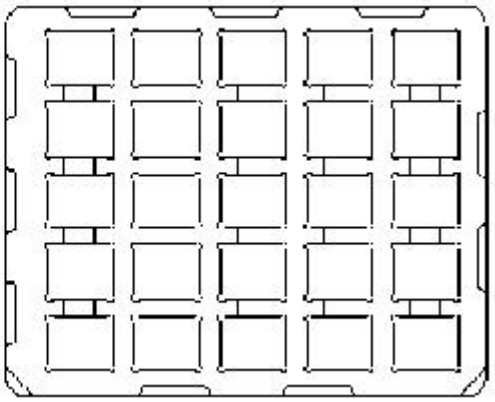
size ： 350*350*35mm

The packing case size:350*210*370mm

11.4 Tray

Use pallet packaging for less than 300 pieces





12. Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH)

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more