FN-LINK欧智通

3181A-S

Wi-Fi Single-band 1X1 802.11b/g/n

SDIO Module Datasheet

3181A-S Module Datasheet

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_____ Signature

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Revision History

Version	Date	Revision Content	Draft	Approved
1.0	2020/08/22	New version	Lxy	Szs
1.1	2021/03/19	Update material list	Lxy	Szs
1.2	2021/05/10	Added non shielding type height information	Lxy	Szs
1.3	2021/08/21	Update Carrier Tape	LXY	QJP
1.4	2021/10/21	Add FG3181ASXX-03 P/N	LXY	QJP

CONTENTS

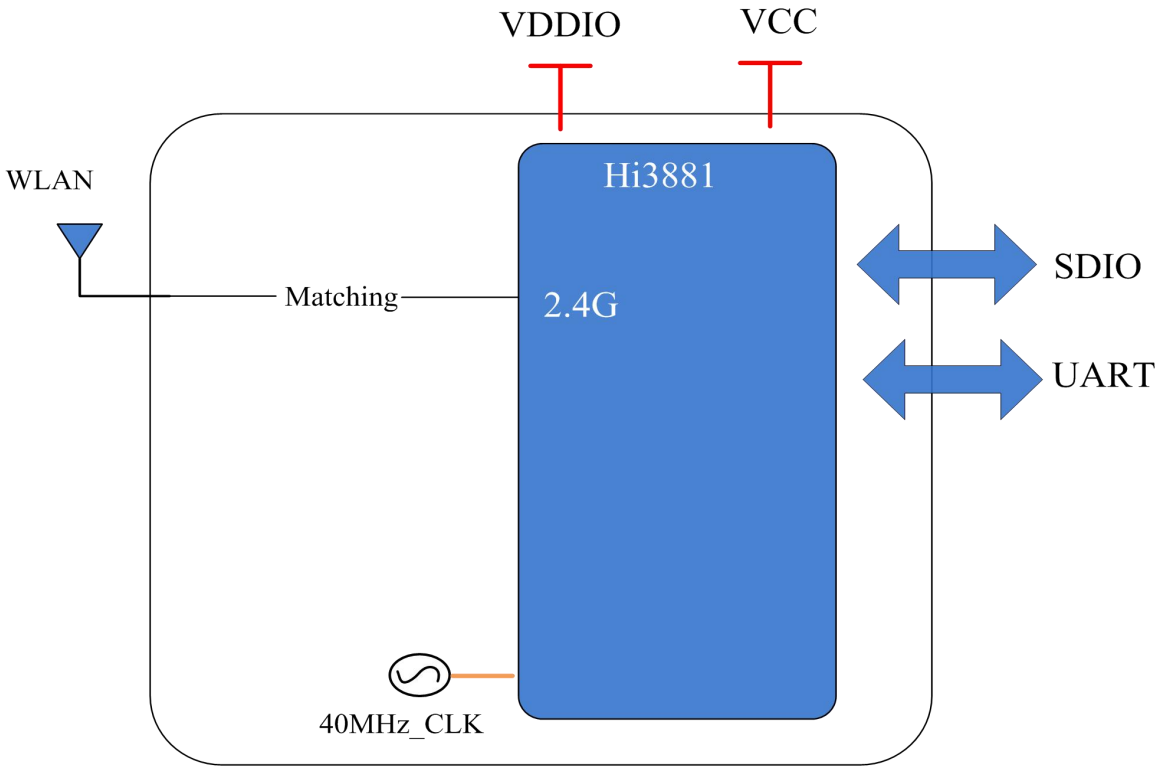
1 Overview

1.1 Introduction

3181A-S is a highly integrated 2.4 GHz Wi-Fi module that support the IEEE 802.11b/g/n baseband and RF circuit. It supports 20 MHz standard bandwidth and 5 MHz/10 MHz narrow bandwidth, and provides a physical layer rate up to 72.2 Mbit/s. Wi-Fi baseband supports the orthogonal frequency division multiplexing (OFDM) technology and is backward compatible with the direct sequence spread spectrum (DSSS) and complementary code keying (CCK) technologies, offering various data rates defined in the IEEE 802.11 b/g/n protocol.

Module chipset including the SPI, UART, I2C, PWM, GPIO, and multi-channel ADC. In addition, it provides high-speed SDIO2.0 slave interfaces, with clock frequency up to 50 MHz.

Block Diagram:



1.2 Features

- Operate at ISM frequency bands (2.4GHz)
- Maximum rate of 72.2 Mbit/s@HT20 MCS7
- SDIO interface for Wi-Fi

- High transmitting power
- High receiving sensitivity
- PHY supporting IEEE 802.11b/g/n
- MAC supporting IEEE802.11 d/e/h/i/k/v/w
- WFA WPA, WFA WPA2 personal, and WPS2.0 for Wi-Fi

1.3 General Specification

Model Name	3181A-S
Product Description	Support Wi-Fi functionality
Dimension	L x W x H: 12 x 12 x2.3 mm -with shielding 12 x 12 x1.7 mm -non shielding
Wi-Fi Interface	Support SDIO
Ambient temperature	-40°C to 85°C
Storage temperature	-40°C to 85°C
RoHS	All hardware components are fully compliant with EU RoHS directive

1.4 Recommended Operating Rating

		Min.	Typ.	Max.	Unit
Ambient temperature		-40	25	85	deg.C
VCC		2.3	3.3	3.6	V
VDDIO		-	1.8V/3.3V	-	V
Power Consumption		VCC = 3.3V(Unit:mA)			
	-	-			
	TX Test mode (2.4G HT20@17dbm)	288			
	RX Test mode (2.4G HT20)	53			

Note: Suggested power input range in 3.3V. Extreme operating conditions will degrade the EVM performance.

2 Wi-Fi RF Specification

2.1 2.4GHz RF Specification

Feature	**Description**			
WLAN Standard	IEEE 802.11 b/g/n Wi-Fi compliant			
Frequency Range	2.400～2.4835GHz			
Number of Channels	**Wi-Fi:** US: channel 1~11; EU: channel 1~13; Japan: channel 1~14;			
Spectrum Mask	Min. b/g/n	Typ. b/g/n	Max. b/g/n	Unit b/g/n
1st side lobes(to fc ± 11MHZ)	-	-43/-30/-40	-	dBr
2st side lobes(to fc ± 22MHZ)	-	-52/-33/-58	-	dBr
Freq. Tolerance	-20/-20/-20	-	20/20/20	ppm

Test Items	**Typical Value**	**EVM**
Output Power[1]	802.11b /11Mbps : 15dBm ± 1.5 dB	EVM ≤ -10dB
	802.11g /54Mbps : 15dBm ± 1.5 dB	EVM ≤ -25dB
	802.11n /MCS7 : 15dBm ± 1.5 dB	EVM ≤ -28dB

Test Items	**Test Value**	**Standard Value**
SISO Receive Sensitivity (11b,20MHz) @8% PER	- 1Mbps PER @ -97 dBm	≤-94 dBm
	- 2Mbps PER @ -95 dBm	≤-92 dBm
	- 5.5Mbps PER @ -92 dBm	≤-89 dBm
	- 11Mbps PER @ -90 dBm	≤-87 dBm
SISO Receive Sensitivity (11g,20MHz) @10% PER	- 6Mbps PER @ -94 dBm	≤-89 dBm
	- 9Mbps PER @ -92 dBm	≤-88 dBm
	- 12Mbps PER @ -91 dBm	≤-87 dBm
	- 18Mbps PER @ -88 dBm	≤-86 dBm
	- 24Mbps PER @ -85 dBm	≤-84 dBm
	- 36Mbps PER @ -82 dBm	≤-80 dBm
	- 48Mbps PER @ -79 dBm	≤-77 dBm
	- 54Mbps PER @ -77 dBm	≤-75 dBm
SISO Receive Sensitivity (11n,20MHz) @10% PER	- MCS=0 PER @ -93 dBm	≤-89 dBm
	- MCS=1 PER @ -90 dBm	≤-86 dBm
	- MCS=2 PER @ -89 dBm	≤-84 dBm
	- MCS=3 PER @ -85 dBm	≤-82 dBm
	- MCS=4 PER @ -82 dBm	≤-79 dBm

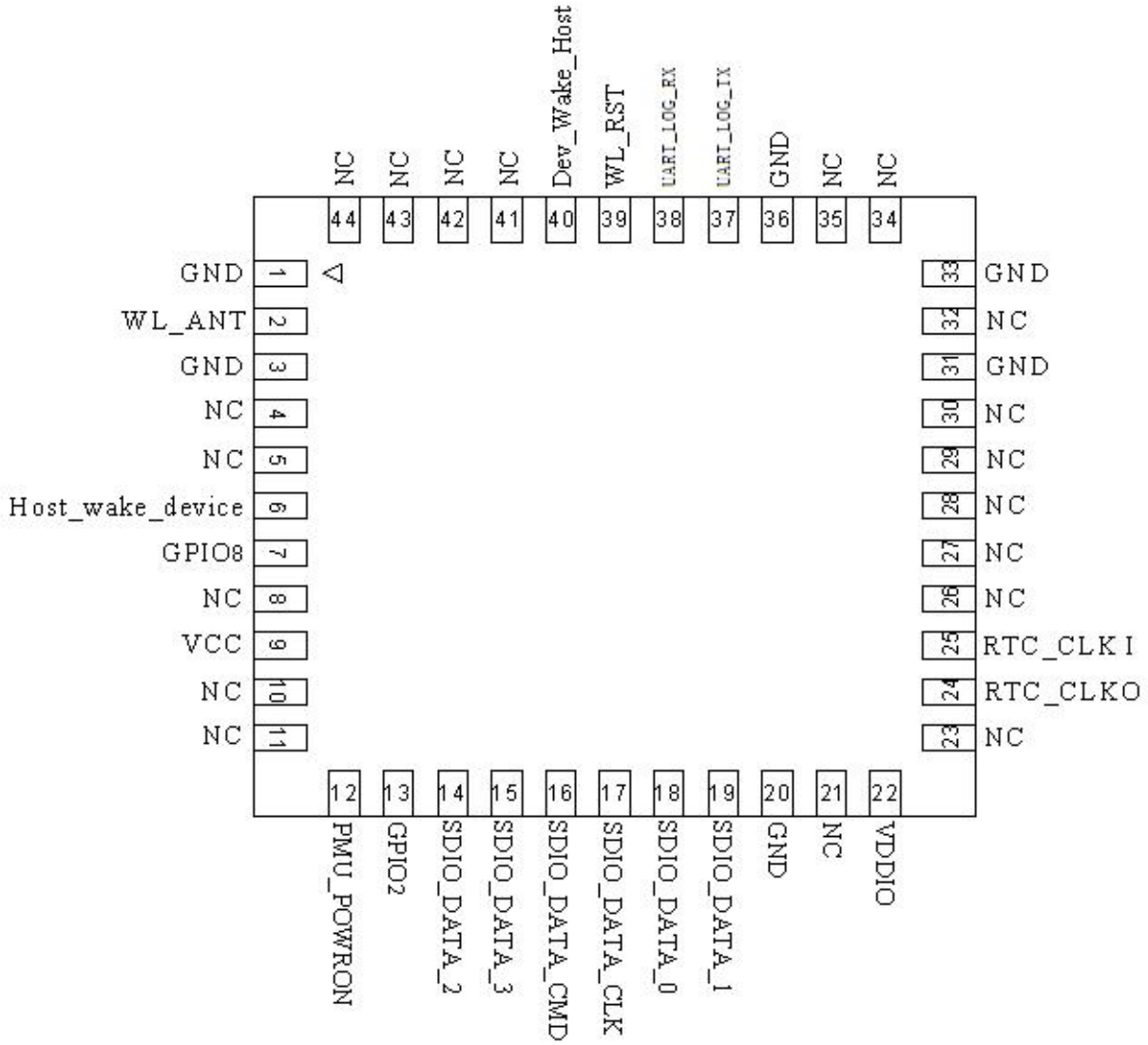
	- MCS=5	PER @ -78 dBm	≤-76 dBm
	- MCS=6	PER @ -76 dBm	≤-74 dBm
	- MCS=7	PER @ -73 dBm	≤-72 dBm
Maximum Input Level	802.11b: -10 dBm		
	802.11g/n: -20 dBm		
Antenna Reference	PCB antenna with 0~2 dBi peak gain		

1. All rate power is control by firmware driver of wifi_cfg file.

3 Pin Assignments

3.1 Pin Outline

<TOP VIEW>



3.2 Pin Definition

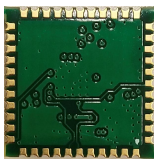
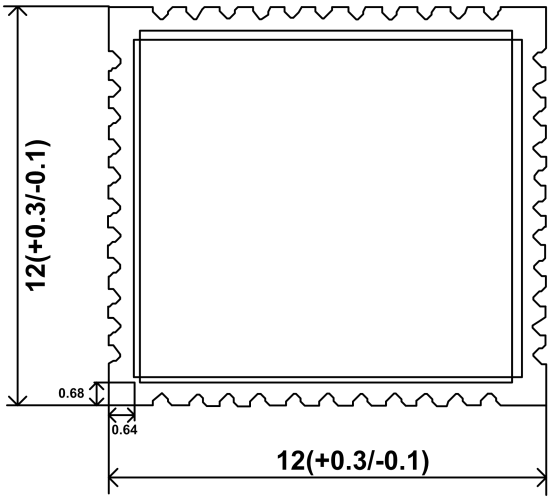
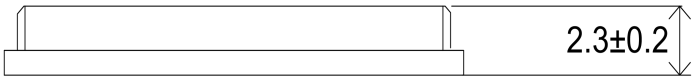
NO	Name	Type	Description	Voltage
1	GND	—	Ground connections	
2	WL_ANT	I/O	RF I/O port	
3	GND	—	Ground connections	
4	NC	—	Floating (Don't connected to ground)	
5	NC	—	Floating (Don't connected to ground)	
6	Host wake device	I	Host Wake up Wi-Fi, GPIO06 (Don't support this function currently)	VDDIO
7	GPIO8	I/O	SDIO interrupt (Floating if not used)	VDDIO
8	NC	—	Floating (Don't connected to ground)	
9	VCC	P	Main power voltage source input 2.3V-3.6V	3.3V
10	NC	—	Floating (Don't connected to ground)	
11	NC	—	Floating (Don't connected to ground)	
12	PMU_POWRON	I	Enable pin for WLAN device Defualt ON: pull high ; OFF: pull low Suggest using this pin shut down module for saving mode	VDDIO
13	GPIO2	I/O	SDIO data interrupt. Or Dev wake host (wake function not supported currently)	VDDIO
14	SDIO_DATA_2	I/O	SDIO data line 2, GPIO09	VDDIO
15	SDIO_DATA_3	I/O	SDIO data line 3, GPIO10	VDDIO
16	SDIO_DATA_CMD	I/O	SDIO command line, GPIO11	VDDIO
17	SDIO_DATA_CLK	I	SDIO clock line, GPIO12	VDDIO
18	SDIO_DATA_0	I/O	SDIO data line 0, GPIO13	VDDIO
19	SDIO_DATA_1	I/O	SDIO data line 1, GPIO14	VDDIO
20	GND	—	Ground connections	
21	NC	—	Floating (Don't connected to ground)	
22	VDDIO	P	I/O Voltage supply input 1.8V/3.3V	VDDIO
23	NC	—	Floating (Don't connected to ground)	
24	RTC_CLK O	I/O	Floating(not used), GPIO00	VDDIO
25	RTC_CLK I	I	Floating(not used), GPIO01	VDDIO
26	NC	—	Floating (Don't connected to ground)	
27	NC	—	Floating (Don't connected to ground)	
28	NC	—	Floating (Don't connected to ground)	

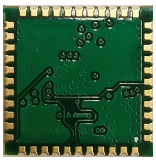
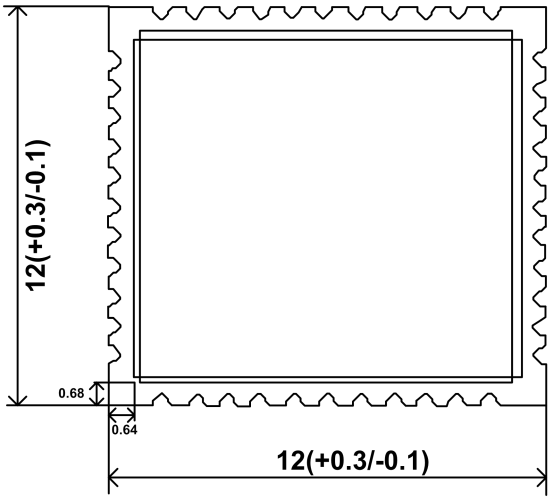
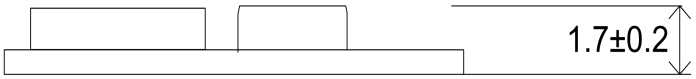
29	NC	—	Floating (Don’t connected to ground)	
30	NC	—	Floating (Don’t connected to ground)	
31	GND	—	Ground connections	
32	NC	—	Floating (Don’t connected to ground)	
33	GND	—	Ground connections	
34	NC	-	Floating (Don’t connected to ground)	
35	NC	—	Floating (Don’t connected to ground)	
36	GND	—	Ground connections	
37	UART_LOG_TX	—	Floating(not used),GPIO03 For debug can floating this pin	VDDIO
38	UART_LOG_RX	—	Floating(not used),GPIO04 For debug can floating this pin	VDDIO
39	WL_RST	I	Wi-Fi reset pin. GPIO07 Low: reset enable, Defualt High: reset disable, (Don’t support this function currently)	VDDIO
40	Dev_Wake_Host	O	Wi-Fi wake up host. GPIO05 (Don’t support this function currently)	VDDIO
41	NC	—	Floating (Don’t connected to ground)	
42	NC	—	Floating (Don’t connected to ground)	
43	NC	—	Floating (Don’t connected to ground)	
44	NC	—	Floating (Don’t connected to ground)	

P:POWER I:INPUT O:OUTPUT

4 Dimensions

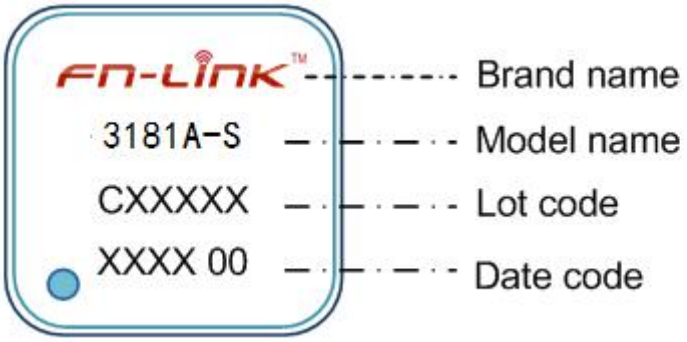
4.1 Module Picture

L x W : 12 x 12 (+0.3/-0.1) mm Shielding version  	
H: 2.3 (±0.2) mm	
Weight	0.57g

L x W : 12 x 12 (+0.3/-0.1) mm Non shielding version  	
H: 1.7 (±0.2) mm	
Weight	0.45g

4.2 Marking Description

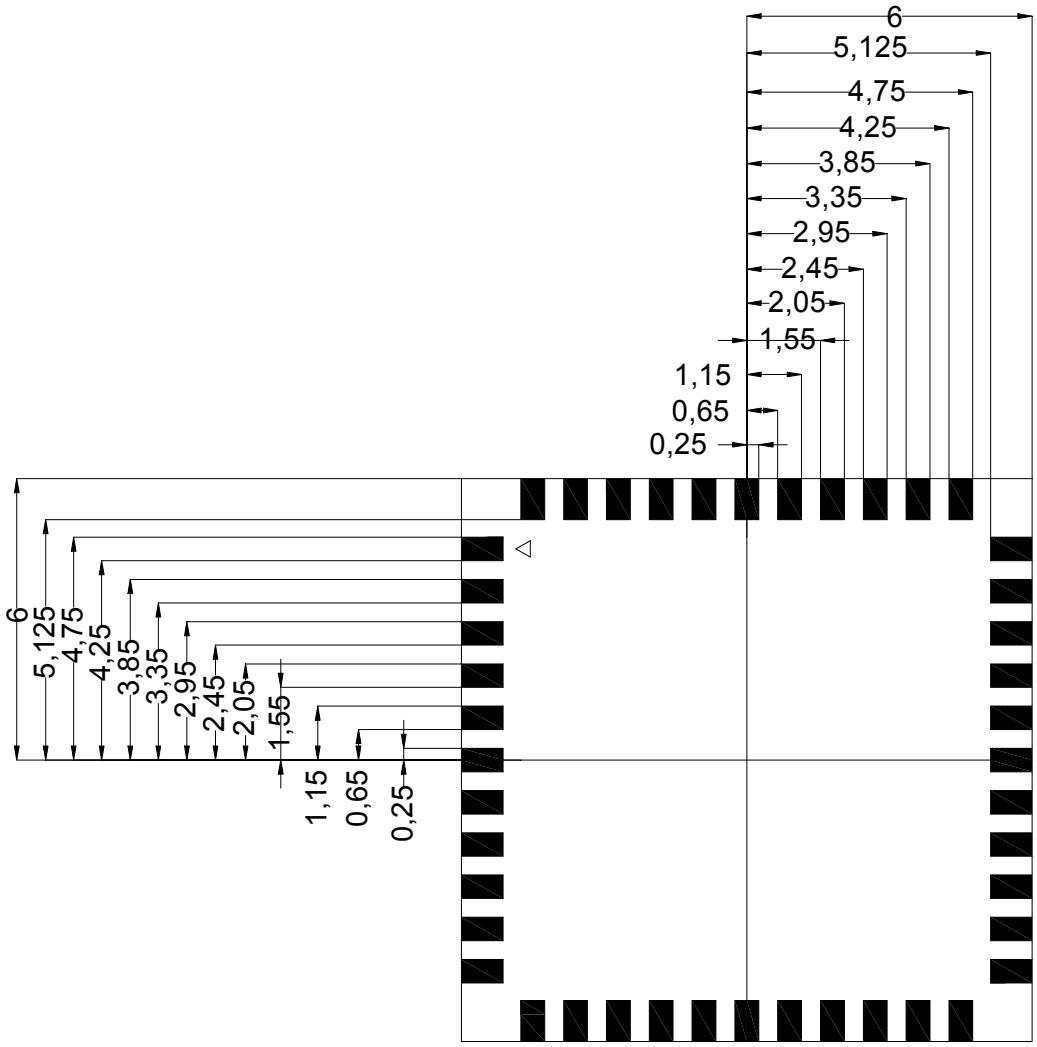
< TOP VIEW >



4.3 Module Physical Dimensions

(Unit: mm)

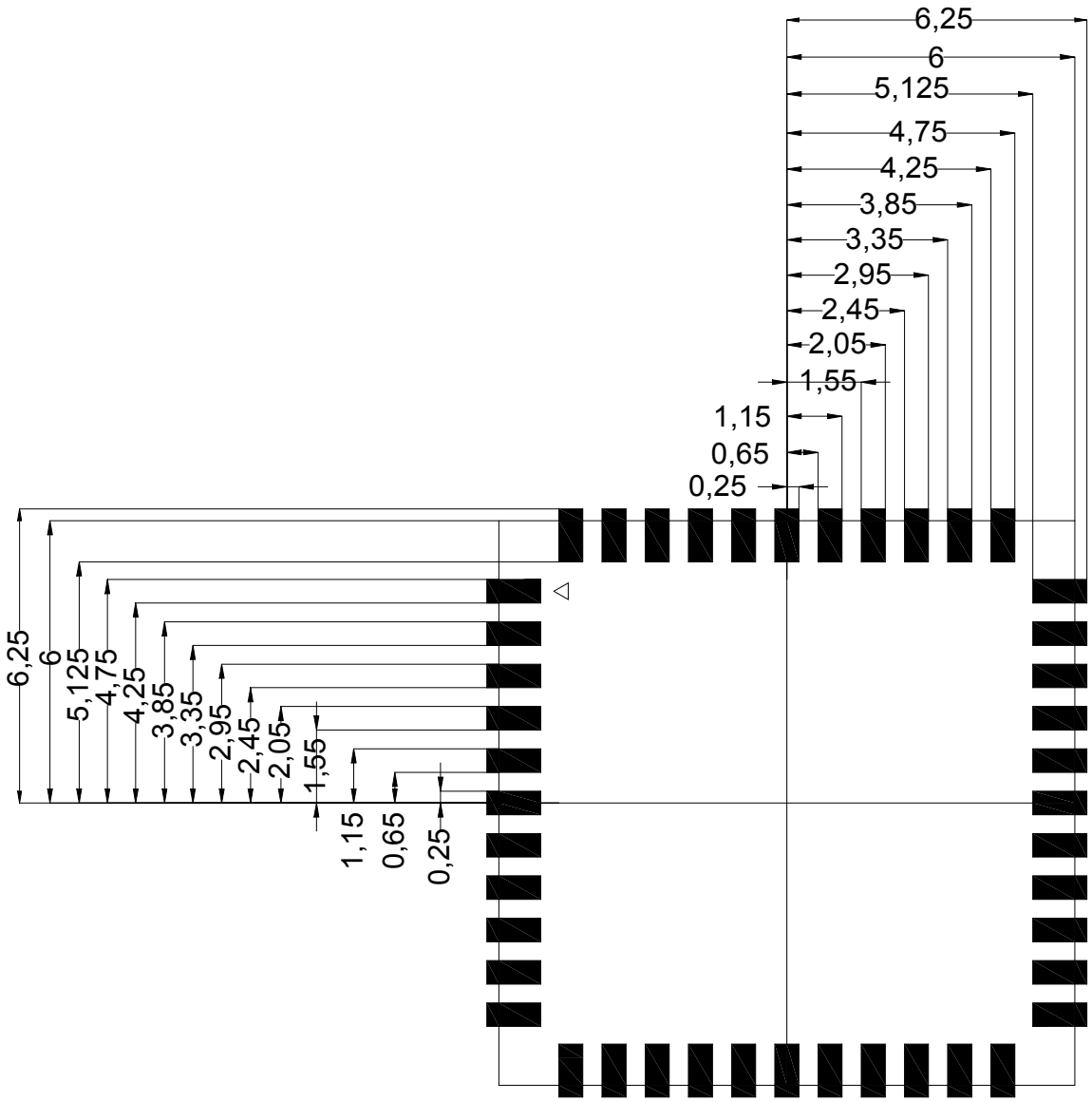
< TOP VIEW >



4.4 Layout Recommendation

(Unit: mm)

< TOP VIEW >



5 Host Interface Timing Diagram

5.1 SDIO Pin Description

The secure digital input/output (SDIO) interface supports three working modes:

Default speed mode (DS)

The maximum frequency of the interface clock is 25 MHz. The interface clock can work in 1-bit or 4-bit mode.

High speed mode (HS)

The maximum frequency of the interface clock is 50 MHz.

SDR25 mode

The maximum frequency of the interface clock is 50 MHz

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1
DATA2	Data Line 2
DATA3	Data Line 3
CLK	Clock
CMD	Command Line

5.2 SDIO CLK Timing Diagram

DS Mode

The DS mode is the default mode after the SDIO is powered on. To ensure compatibility with various host components, the DS mode requires a low working rate and supports only the 25 MHz clock.

Clock parameters in DS mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	25	MHz	$C_{CARD} \leq 10$ pF
Clock frequency Identification Mode	f_{OD}	-	400	kHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	17	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	17	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	3	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	3	ns	$C_{CARD} \leq 10$ pF

Clock parameters in DS mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	25	MHz	$C_{CARD} \leq 10$ pF
Clock frequency Identification Mode	f_{OD}	-	400	kHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	14	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	14	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	6	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	6	ns	$C_{CARD} \leq 10$ pF

Figure 8-6 shows the output data timing in DS mode. tISU is the setup time, that is, the stability time required by the data of the SDIO interface before clock sampling in this mode. tIH is the hold time, that is, the time required by the data of the SDIO interface to retain the original level after clock sampling in this mode.

Figure 8-6 Input timing in DS mode

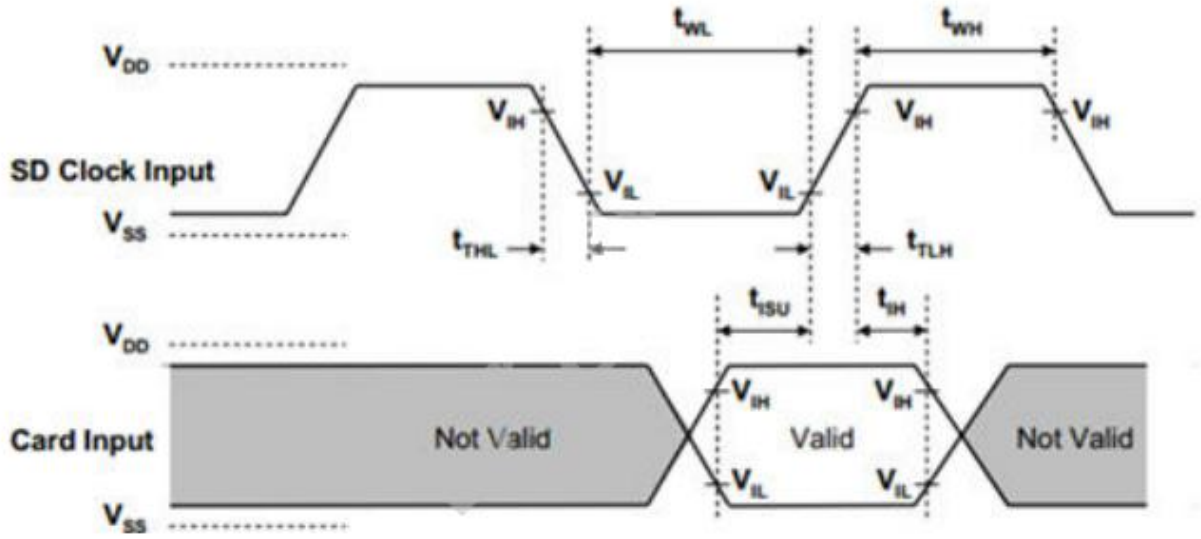


Figure 8-7 shows the input data timing in DS mode. Where, tODLY(max) is the maximum delay of the output data relative to the clock falling edge, and tODLY(min) is the minimum delay of the output data relative to the clock falling edge.

Figure 8-7 Output timing in DS mode

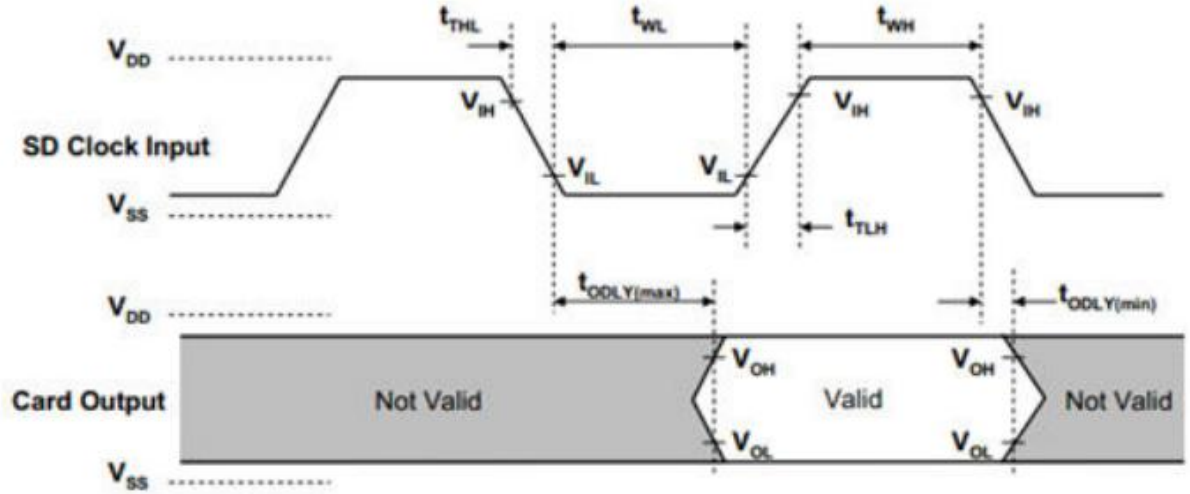


Table 8-12 describes the timing restrictions in DS mode.

Table 8-12 Timing restrictions in DS mode

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	11	ns	$C_L \leq 40$ pF
Output Delay time during Identification Mode	t_{ODLY}	-	11	ns	$C_L \leq 40$ pF

Note: In DS mode, the output data is referenced to the clock falling edge, and the input data is referenced to the clock rising edge.

HS Mode

The HS mode is entered after the SDIO is powered on and initialized because a higher working rate than the DS mode is required. In HS mode, the clock supports 50 MHz. For details about the restrictions on the clock, see **Table 8-13**.

Table 8-13 Clock parameters in HS mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	7	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	7	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	3	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	3	ns	$C_{CARD} \leq 10$ pF

Table 8-14 Clock parameters in HS mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	4	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	4	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	6	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	6	ns	$C_{CARD} \leq 10$ pF

Figure 8-8 shows the input data timing in HS mode. tISU is the setup time, that is, the stability time required by the data of the SDIO interface before clock sampling in this mode. tIH is the hold time, that is, the time required by the data of the SDIO interface to retain the original level after clock sampling in this mode

Figure 8-8 Input timing in HS mode

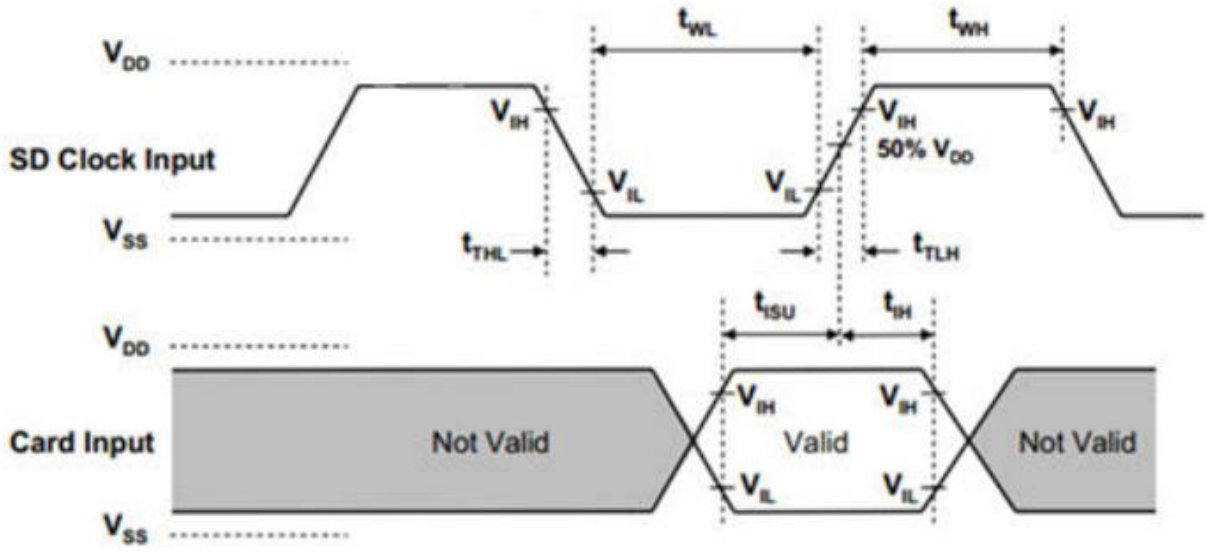


Figure 8-9 shows the input data timing in HS mode. Where, tODLY(max) is the maximum delay of the output data relative to the clock rising edge, and tOH is the minimum delay of the output data relative to the clock rising edge.

Figure 8-9 Output timing in HS mode

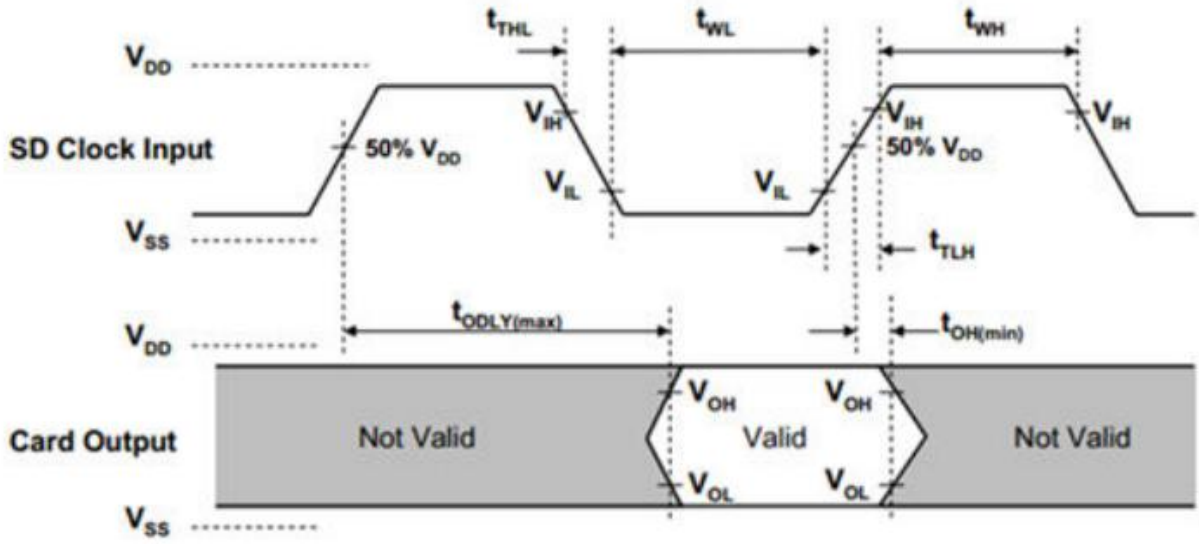


Table 8-15 describes the timing restrictions in HS mode.

Table 8-15 Timing restrictions in HS mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	12	ns	$C_L \leq 40$ pF
Output Hold time	t_{OH}	3	-	ns	$C_L \leq 40$ pF
Total System Capacitance for each line	C_L	-	40	pF	1 card

Table 8-16 Timing restrictions in HS mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	18	ns	$C_L \leq 40$ pF
Output Hold time	t_{OH}	4.5	-	ns	$C_L \leq 40$ pF
Total System Capacitance for each line	C_L	-	40	pF	1 card

Note: The data signal timing in HS mode is different from that in DS mode. The output data and input data are referenced to the clock rising edge.

SDR25 Mode

The SDR25 mode is entered only after the voltage of the SDIO is switched. In this mode, the maximum interface clock frequency is 50 MHz. **Table 8-17** describes the clock restrictions.

Table 8-17 Clock parameters in SDR25 mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	7	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	7	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	3	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	3	ns	$C_{CARD} \leq 10$ pF

Table 8-18 Clock parameters in SDR25 mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Clock CLK (All values are referenced to min(V_{IH}) and max(V_{IL}))					
Clock frequency Date Transfer Mode	f_{PP}	-	50	MHz	$C_{CARD} \leq 10$ pF
Clock low time	t_{WL}	4	-	ns	$C_{CARD} \leq 10$ pF
Clock high time	t_{WH}	4	-	ns	$C_{CARD} \leq 10$ pF
Clock rise time	t_{TLH}	-	6	ns	$C_{CARD} \leq 10$ pF
Clock fall time	t_{THL}	-	6	ns	$C_{CARD} \leq 10$ pF

Table 8-19 Timing restrictions in SDR25 mode (VDDIO = 3.3 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	12	ns	$C_L \leq 40$ pF
Output Hold time	t_{OH}	3	-	ns	$C_L \leq 40$ pF
Total System Capacitance for each line	C_L	-	40	pF	1 card

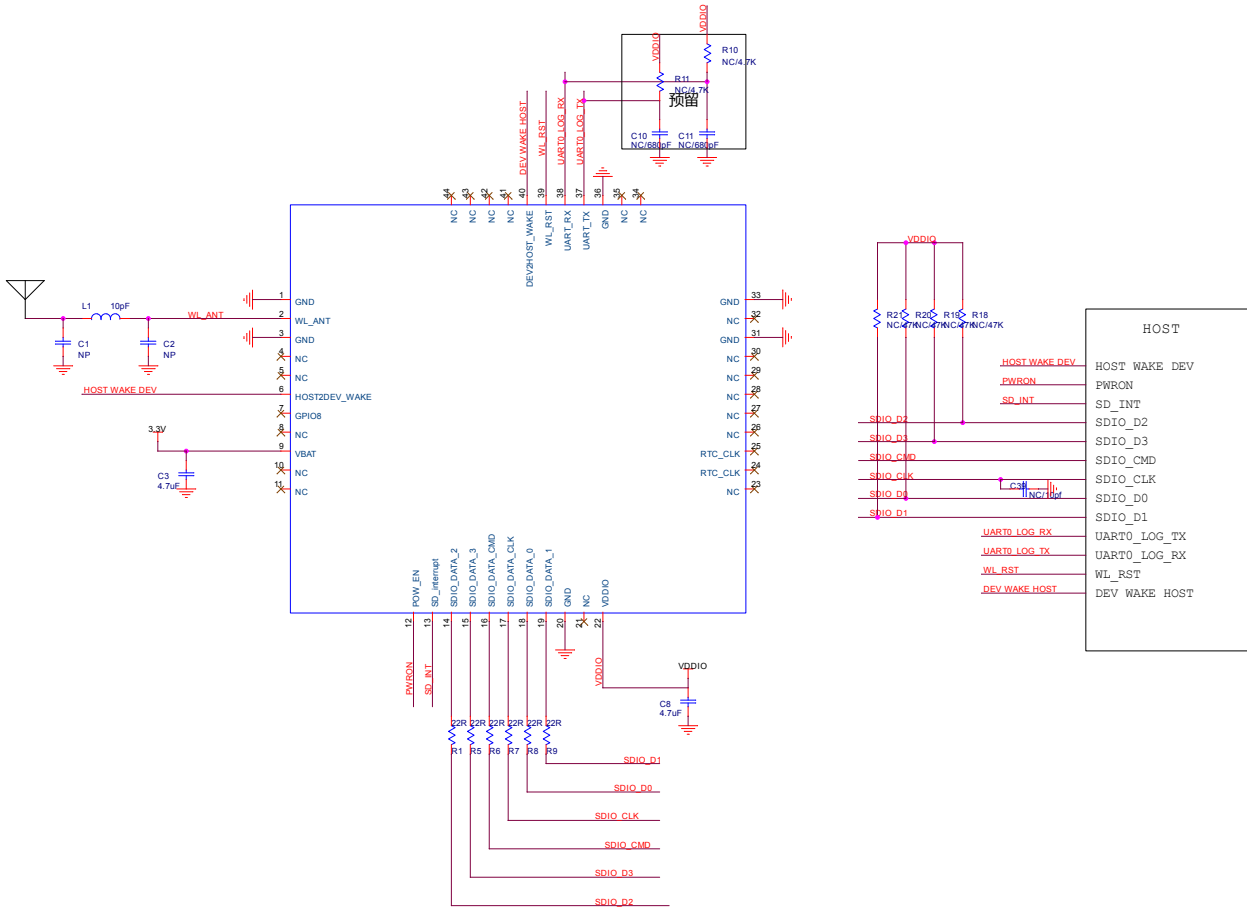
Table 8-20 Timing restrictions in SDR25 mode (VDDIO = 1.8 V)

Parameter	Symbol	Min.	Max.	Unit	Remarks
Inputs CMD, DAT (referenced to CLK)					
Input set-up time	t_{ISU}	3.5	-	ns	$C_{CARD} \leq 10$ pF
Input hold time	t_{IH}	0	-	ns	$C_{CARD} \leq 10$ pF
Outputs CMD, DAT(referenced to CLK)					
Output Delay time during Data Transfer Mode	t_{ODLY}	-	18	ns	$C_L \leq 40$ pF
Output Hold time	t_{OH}	4.5	-	ns	$C_L \leq 40$ pF
Total System Capacitance for each line	C_L	-	40	pF	1 card

6 Reference Design

6.1 Low Power Dissipation Reference Design

6.2 Normal Power dissipation Reference Design



7 Ordering Information

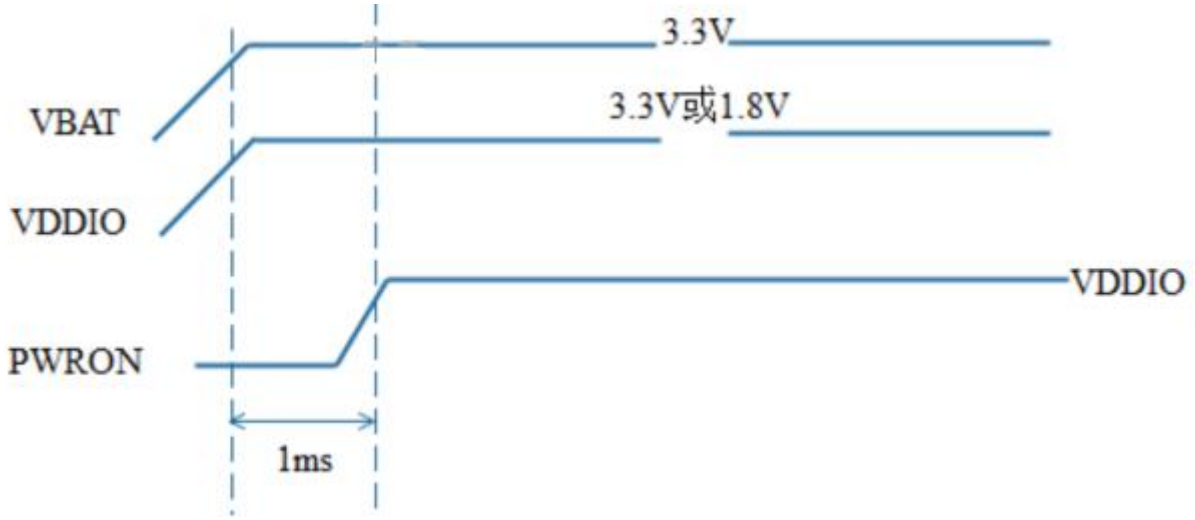
Part No.	Description
FG3181ASXX-00	Hi3881, b/g/n Wi-Fi, 1T1R, 12X12mm, SDIO, PCB V1.0 Halogen Free,with shielding,TVS.
FG3181ASXX-01	Hi3881, b/g/n Wi-Fi, 1T1R, 12X12mm, SDIO, PCB V1.0 Halogen Free,no shielding, LDO,TVS,all cap
FG3181ASXX-02	Hi3881, b/g/n Wi-Fi, 1T1R, 12X12mm, SDIO, PCB V1.0 Halogen Free,no shielding, LDO,TVS,all cap

FG3181ASXX-K0	Hi3881, b/g/n Wi-Fi, 1T1R, 12X12mm, SDIO, PCB V1.0 Halogen Free,with shielding.LDO,TVS,客供 IC 版
FG3181ASXX-03	Hi3881,b/g/n ,1T1R,12X12mm ,SDIO2.0,无屏蔽盖,LDO 版,（new HDK)

8 The Key Material List

Inductor	2016,2.2uH,±20%,DCR=0.125ohm,Isat=1.5A,Irms=1.5A	Mirogate,Sunlord,cenke,ceaiya
Shielding cover	3161A-IL,V1.0,shielding,10.45x10.45x1.5mm T=0.15mm	信太,精力通
PCB	3161A-SL,green,4L,FR4,Tg150,Au,12X12X0.8mm	XY-PCB,KX-PCB,SL-PCB,sunlord
Crystal	2520,40MHZ,13.8PF,7ppm	HOSONIC,ECEC,JWT,TKD
Chipset	Hi3881RNIV100 ,WiFi ,802.11b/g/n,SDIO,UART，QFN32, 5x5mm	Hisilicon
TVS	0201,4V, 0.05pF ,15KV TVS	Murata,Sunlord,way-on

9 Power on Sequence



※ VCC / VDDIO supreme electrical order requirements

※ In the process of power up, GPIO02 internal weak pull low ,the 40MHz crystal is selected..

10 Design Attention

1. PMU_PWRON is enable pin of the module. Default is pull high.

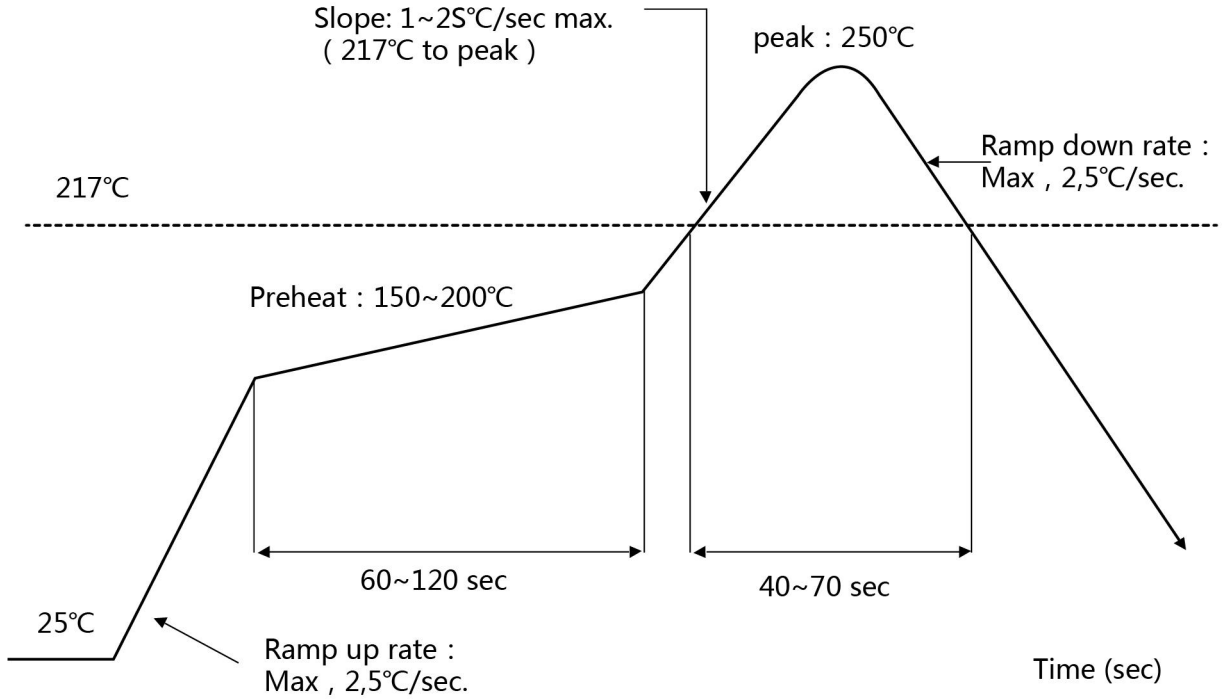
2. Wake function may not supported with recently applications, for power saving please using POWER EN pin enable or disable the module.

11 Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

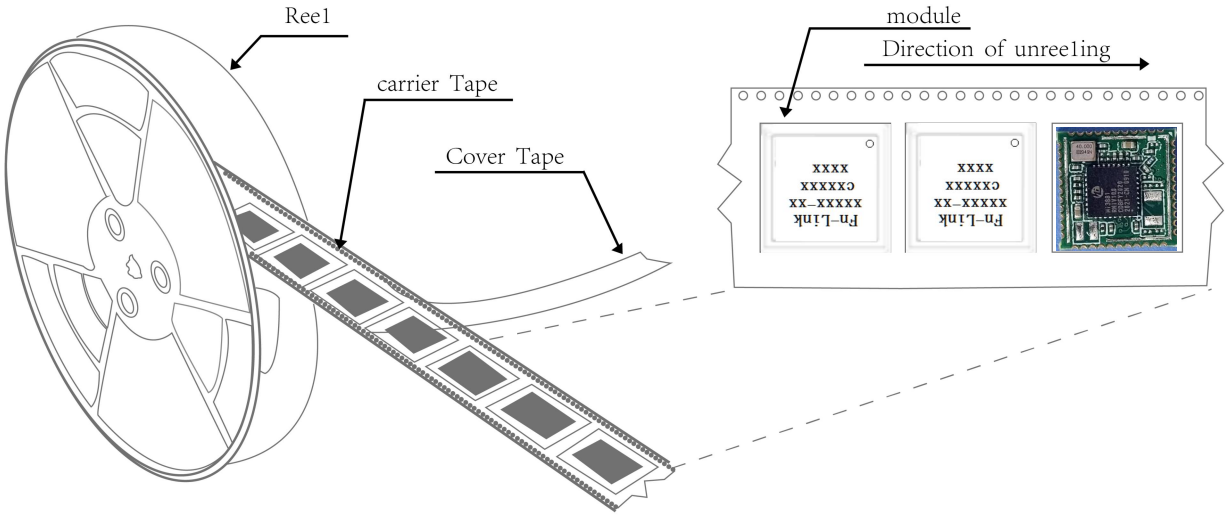
Number of Times : ≤2 times



12 Packing Information

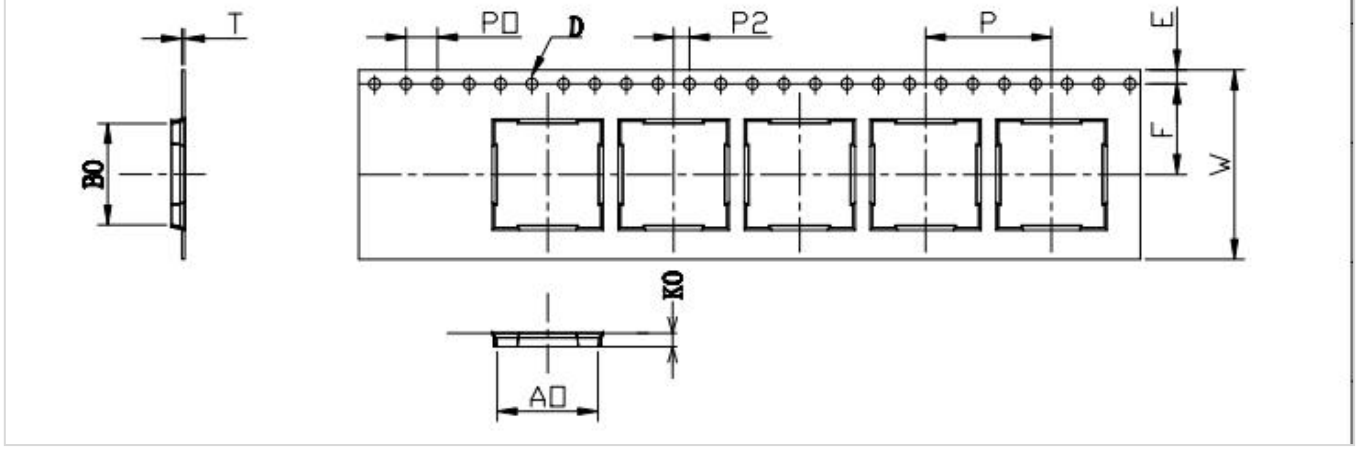
12.1 Reel

A roll of 1500pcs

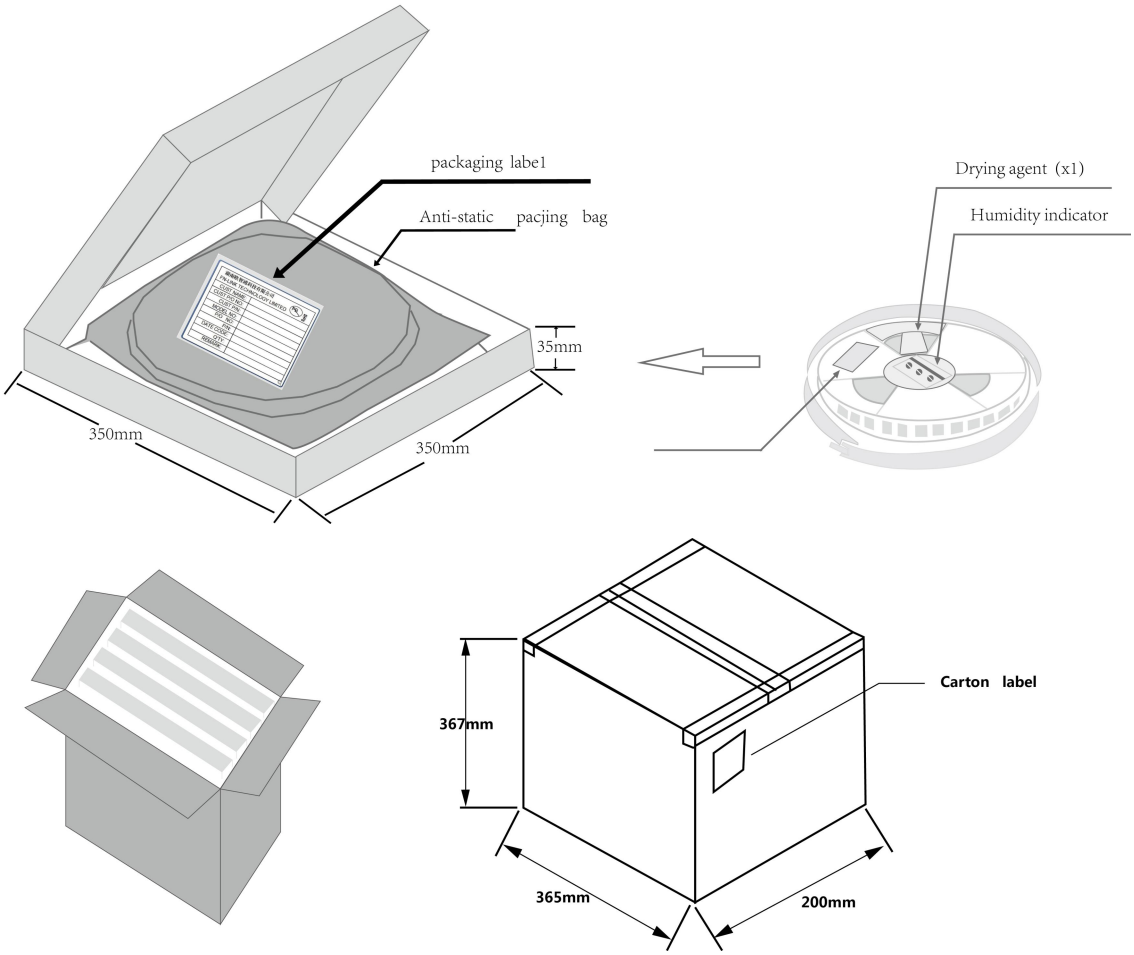


12.2 Carrier Tape Detail

ITEM	W	A0	B0	D	F	E	K0	P0	P2	P	T
DIM	24	12.45	12.45	1.50	11.5	1.75	2.60	4.0	2.0	16.0	0.30
TOLE	+0.3 -0.3	±0.10	±0.10	+0.1 -0.0	+0.1 -0.1	±0.1	±0.10	±0.1	±0.1	±0.1	±0.05



12.3 Packaging Detail



12.4 Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care
all the relatives requirements for using this kind of components.
Moreover, the customer has to take care of the following conditions:
a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).
b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.
c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition
b) “IPC/JEDEC J-STD-033A paragraph 5.2” is respected
d) Baking is required if conditions b) or c) are not respected
e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more