# K255B-SR

**Wi-Fi Dual-band 1X1 11a/b/g/n/ac +Bluetooth 5.0 Combo Module Datasheet**

# K255B-SR Module Datasheet

**Office:** 6 Floor, Building U6, Junxiang U8 Park,
Hangcheng Avenue, Bao'an District,
Shenzhen City, CHINA
**Factory:** No.8, Litong Road, Liuyang Economic & Technical
Development Zone, Changsha, Hunan, CHINA
**TEL:** +86-755-2955-8186
**Website:** www.fn-link.com

Customer Approval : _____ Company

_____ Title

_____ Signature

_____ Date

_____ Fn-Link

# Revision History

| Version | Date | Revision Content | Draft | Approved |
|---------|------|------------------|-------|----------|
| 1.0 | 2021/02/23 | Draft version | Lgp | Szs |
| 2.0 | 2021/03/18 | Correct typo; Update RF specification; Update Pin definition; Add module picture | Lgp | Szs |
| 3.0 | 2021/04/12 | Update marking description | Lgp | Szs |
| 4.0 | 2021/05/20 | Update RF specification; Update module picture | Lgp | Szs |
| 5.0 | 2021/05/21 | Add general version module info | Lgp | Szs |
| 6.0 | 2021/07/27 | Update bluetooth standards | Tzq | Qjp |
| 7.0 | 2021/09/17 | Update recommended furnace temperature | Tzq | Qjp |

# CONTENTS

# 1 Overview

## 1.1 Introduction

K255B-SR support 1-stream 802.11a/b/g/n/ac solution with MU-MIMO STA mode with Bluetooth smart ready controller, SDIO 3.0 interface, HS-UART mixed interface. It combines WLAN MAC, a 1T1R WLAN baseband, RF in a single chip.

Module complies with IEEE 802.11 a/b/g/n/ac standard and the speed can achieve up to 80MHz bandwidth and PHY data rate of 433Mbps.

Module complies with Bluetooth core specification V5.0, support both classic BDR/EDR and BLE mode.

## 1.2 Features

- CMOS MAC, Baseband PHY and RF in a single chip for IEEE 802.11 a/b/g/n/ac
- Support 802.11ac 1x1, compliant with MU-MIMO STA mode
- SDIO 3.0 interface for WLAN, with rate up to 208MHz
- 802.11ac support maximum rate up to 433Mbps in 80MHz bandwidth
- Support HS-UART and PCM host interface for BT
- Supports Bluetooth V5.0 features
- Dual mode BT 5.0 supporting BDR, EDR, LE1M, LE2M and LE8S rates

# Block Diagram:
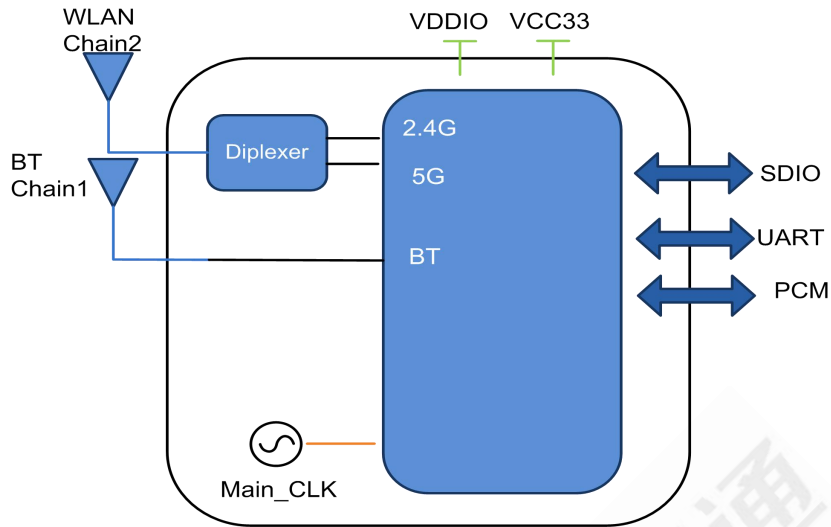


## 1.3 General Specification

| Model Name | K255B-SR |
|---|---|
| Product Description | Support Wi-Fi/Bluetooth functionalities |
| Dimension | L x W x H: 15 x 13 x 2.15 mm (typical) |
| Wi-Fi Interface | Support SDIO 3.0 |
| BT Interface | UART / PCM |
| Operating temperature | 0°C to 70°C |
| Storage temperature | -40°C to 85°C |

## 1.4 Recommended Operating Rating

|  | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|
| Operating Temperature | 0 | 25 | 70 | deg.C |
| VCC33 | 3.15 | 3.3 | 3.45 | V |
| VDDIO | 1.62 | 1.8 | 1.98 | V |

## ※1.5 EEPROM Information

WI-FI

| ID | TBD |
|---|---|

# 2 Wi-Fi RF Specification

## 2.1 2.4GHz RF Specification

| Feature | Description | | | |
|---|---|---|---|---|
| WLAN Standard | IEEE 802.11 b/g/n Wi-Fi compliant | | | |
| Frequency Range | 2.400 GHz ~ 2.4835 GHz (2.4 GHz ISM Band) | | | |
| Number of Channels | 2.4GHz：Ch1 ~ Ch14 | | | |
| Spectrum Mask | Min. b/g/n | Typ. b/g/n | Max. b/g/n | Unit b/g/n |
| 1st side lobes(to fc ± 11MHZ) | - | -43/-30/-40 | - | dBr |
| 2st side lobes(to fc ± 22MHZ) | - | -52/-33/-58 | - | dBr |
| Freq. Tolerance | -20/-20/-20 | - | 20/20/20 | ppm |

| Test Items | Typical Value | EVM |
|---|---|---|
| Output Power | 802.11b /11Mbps: 15dBm ± 2.0 dB | EVM ≤ -9dB |
| | 802.11g /54Mbps: 16dBm ± 2.0 dB | EVM ≤ -25dB |
| | 802.11n /MCS7(HT20): 15dBm ± 2.0 dB | EVM ≤ -28dB |
| | 802.11n /MCS7(HT40): 14dBm ± 2.0 dB | EVM ≤ -28dB |

| Test Items | TYP Test Value | | Standard Value |
|---|---|---|---|
| SISO Receive Sensitivity (11b,20MHz) @8% PER | - 1Mbps | ≤ -92 dBm | ≤ -85 dBm |
| | - 11Mbps | ≤ -82 dBm | ≤ -76 dBm |
| SISO Receive Sensitivity (11g,20MHz) @10% PER | - 6Mbps | ≤ -88 dBm | ≤ -82 dBm |
| | - 54Mbps | ≤ -71 dBm | ≤ -65 dBm |
| SISO Receive Sensitivity (11n,20MHz) @10% PER | - MCS=0 | ≤ -87 dBm | ≤ -82 dBm |
| | - MCS=7 | ≤ -69 dBm | ≤ -64 dBm |
| SISO Receive Sensitivity (11n ,40MHz) @10% PER | - MCS=0 | ≤ -84 dBm | ≤ -79 dBm |
| | - MCS=7 | ≤ -66 dBm | ≤ -61 dBm |
| Maximum Input Level | 802.11b: -10 dBm | | |
| | 802.11g/n: -20 dBm | | |
| Antenna Reference | Small antennas with 0~2 dBi peak gain | | |

## 2.2 5GHz RF Specification

| Feature | Description | |
|---|---|---|
| WLAN Standard | IEEE 802.11a/n/ac 1x1, Wi-Fi compliant | |
| Frequency Range | 5.150 GHz ~ 5.850 GHz (5.0 GHz Band) | |
| Number of Channels | 5.0GHz：Please see the table[1] | |
| **Test Items** | **Typical Value** | **EVM** |
| Output Power | 802.11a /54Mbps:<br>14 dBm ± 2.0 dB | EVM ≤ -25dB |
| | 802.11n /MCS7(HT20):<br>14dBm ± 2.0 dB | EVM ≤ -28dB |
| | 802.11n /MCS7(HT40):<br>13dBm ± 2.0 dB | EVM ≤ -28dB |
| | 802.11ac /MCS8(vHT20):<br>13 dBm ± 2.0 dB | EVM ≤ -30dB |
| | 802.11ac /MCS9(vHT40):<br>12dBm ± 2.0 dB | EVM ≤ -32dB |
| | 802.11ac /MCS9(vHT80):<br>11 dBm ± 2.0 dB | EVM ≤ -32dB |
| **Test Items** | **Test Value** | **Standard Value** |
| Receive Sensitivity (11a, 20MHz) @10% PER | - 6Mbps ≤ -88 dBm | ≤ -82 dBm |
| | - 54Mbps ≤ -70 dBm | ≤ -65 dBm |
| Receive Sensitivity (11n,20MHz) @10% PER | - MCS=0 ≤ -87 dBm | ≤ -82 dBm |
| | - MCS=7 ≤ -69 dBm | ≤ -64 dBm |
| Receive Sensitivity (11n,40MHz) @10% PER | - MCS=0 ≤ -84 dBm | ≤ -79 dBm |
| | - MCS=7 ≤ -66 dBm | ≤ -61 dBm |
| Receive Sensitivity (11ac,20MHz) @10% PER | - MCS=0 ≤ -86 dBm | ≤ -82 dBm |
| | - MCS=8 ≤ -65 dBm | ≤ -59 dBm |
| Receive Sensitivity (11ac,40MHz) @10% PER | - MCS=0 ≤ -83 dBm | ≤ -79 dBm |
| | - MCS=9 ≤ -58 dBm | ≤ -54 dBm |
| Receive Sensitivity (11ac,80MHz) @10% PER | - MCS=0 ≤ -81 dBm | ≤ -76 dBm |
| | - MCS=9 ≤ -55 dBm | ≤ -51 dBm |
| Maximum Input Level | 802.11a/n: -30 dBm | |
| Antenna Reference | Small antennas with 0~2 dBi peak gain | |

Conditions : VBAT=3.3V ; VDDIO=1.8V ; Temp:25°C

Note: The RF specification will be updated in future version.

### [1]5GHz(20MHz) Channel table

| Band range | Operating Channel Numbers | Channel center frequencies (MHz) |
|---|---|---|
| 5180MHz~5240MHz | 36 | 5180 |
| | 40 | 5200 |
| | 44 | 5220 |
| | 48 | 5240 |
| 5260MHz~5320MHz | 52 | 5260 |
| | 56 | 5280 |
| | 60 | 5300 |
| | 64 | 5320 |
| 5550MHz~5700MHz | 100 | 5500 |
| | 104 | 5520 |
| | 108 | 5540 |
| | 112 | 5560 |
| | 116 | 5580 |
| | 120 | 5600 |
| | 124 | 5620 |
| | 128 | 5640 |
| | 132 | 5660 |
| | 136 | 5680 |
| | 140 | 5700 |
| 5745MHz~5825MHz | 149 | 5745 |
| | 153 | 5765 |
| | 157 | 5785 |
| | 161 | 5805 |
| | 165 | 5825 |

# 3 Bluetooth Specification

## 3.1 Bluetooth Specification

| Feature | Description | | |
|---|---|---|---|
| **General Specification** | | | |
| Bluetooth Standard | Bluetooth V5.0 | | |
| Host Interface | UART | | |
| Antenna Reference | Small antennas with 0~2 dBi peak gain | | |
| Frequency Band | 2402 MHz ~ 2480 MHz | | |
| Number of Channels | 79 channels | | |
| Modulation | GFSK, π/4-DQPSK,8DPSK | | |
| **RF Specification** | | | |
| | **Min.** | **Typical.** | **Max.** |
| Output Power | 1 | 3 | 5 |
| Sensitivity @ BER=0.1% for GFSK (1Mbps) | | | -70 dBm |
| Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps) | | | -70 dBm |
| Sensitivity @ BER=0.01% for 8DPSK (3Mbps) | | | -70 dBm |
| Maximum Input Level | GFSK (1Mbps): -20dBm | | |
| | π/4-DQPSK (2Mbps): -20dBm | | |
| | 8DPSK (3Mbps): -20dBm | | |

Note: The RF specification will be updated in future version.

# 4 Pin Assignments

## 4.1 Pin Outline

< TOP VIEW >
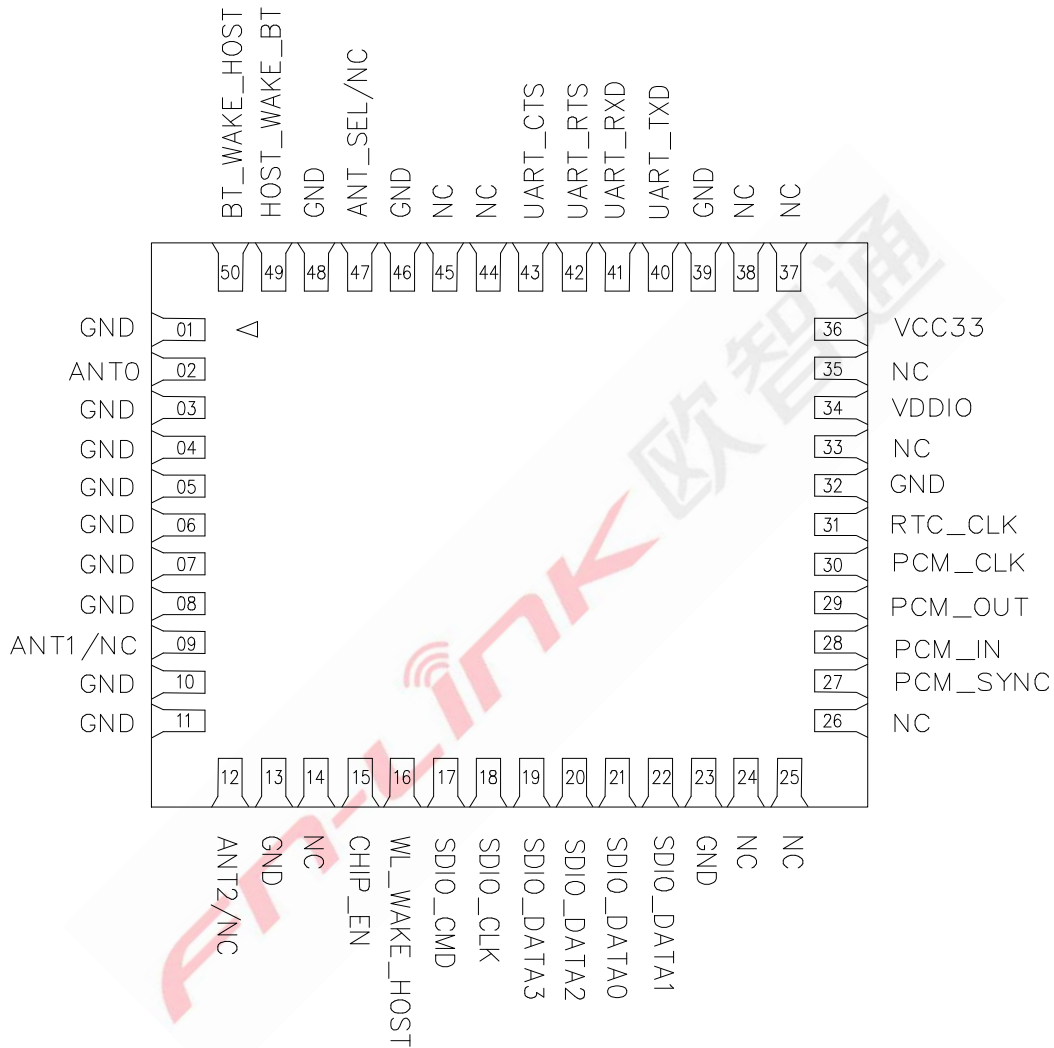


## 4.2 Pin Definition

| NO | Name | Type | Description | Voltage |
|----|------|------|-------------|---------|
| 1 | GND | — | Ground connections | |
| 2 | ANT0 | I/O | RF I/O port for BT | |
| 3 | GND | — | Ground connections | |
| 4 | GND | — | Ground connections | |

| 5 | GND | — | Ground connections | |
|---|---|---|---|---|
| 6 | GND | — | Ground connections | |
| 7 | GND | — | Ground connections | |
| 8 | GND | — | Ground connections | |
| 9 | ANT1/NC | — | Dual band Wi-Fi RF I/O for FGK255BSRX-00; NC for FGK255BSRX-XM | |
| 10 | GND | — | Ground connections | |
| 11 | GND | — | Ground connections | |
| 12 | ANT2/NC | I/O | Dual band Wi-Fi RF I/O for FGK255BSRX-XM; NC for FGK255BSRX-00 | |
| 13 | GND | — | Ground connections | |
| 14 | NC | — | No connect | |
| 15 | CHIP_EN | I | CHIP_EN This pin can externally shut down WLAN function when pulled low, default high | 1.8V |
| 16 | WL_WAKE_HOST | O | WLAN wake-up HOST | 1.8V |
| 17 | SDIO_CMD | I/O | SDIO command line | 1.8V |
| 18 | SDIO_ CLK | I/O | SDIO clock line | 1.8V |
| 19 | SDIO_DATA_3 | I/O | SDIO data line 3 | 1.8V |
| 20 | SDIO_DATA_2 | I/O | SDIO data line 2 | 1.8V |
| 21 | SDIO_DATA_0 | I/O | SDIO data line 0 | 1.8V |
| 22 | SDIO_DATA_1 | I/O | SDIO data line 1 | 1.8V |
| 23 | GND | — | Ground connections | |
| 24 | NC | — | No connect | |
| 25 | NC | — | No connect | |
| 26 | NC | — | No connect | |
| 27 | PCM_SYNC | I/O | PCM sync signal | 1.8V |
| 28 | PCM_IN | I | PCM data input | 1.8V |
| 29 | PCM_OUT | O | PCM Data output | 1.8V |
| 30 | PCM_CLK | I/O | PCM clock | 1.8V |
| 31 | RTC_CLK | I | External Low Power Clock input (32.768KHz) If not used keep NC | |
| 32 | GND | — | Ground connections | |
| 33 | NC | — | No connect | |
| 34 | VDDIO | P | I/O Voltage supply input | 1.8V |
| 35 | NC | — | No connect | |

| 36 | VCC33 | P | Main power voltage source input | 3.3V |
|----|-------|---|----------------------------------|------|
| 37 | NC | — | No connect | |
| 38 | NC | — | No connect | |
| 39 | GND | — | Ground connections | |
| 40 | UART_TXD | O | Bluetooth UART interface | 1.8V |
| 41 | UART_RXD | I | Bluetooth UART interface | 1.8V |
| 42 | UART_RTS_N | O | Bluetooth UART interface | 1.8V |
| 43 | UART_CTS_N | I | Bluetooth UART interface | 1.8V |
| 44 | NC | — | No connect | |
| 45 | NC | — | No connect | |
| 46 | GND | — | Ground connections | |
| 47 | ANT_SEL/NC | O | MUX Uart BT Print Out<br>If not used keep NC | |
| 48 | GND | — | Ground connections | |
| 49 | HOST_WAKE_BT | I | HOST wake-up Bluetooth device<br>The function of this PIN will be updated in future version | 1.8V |
| 50 | BT_WAKE_HOST | O | Bluetooth device to wake-up HOST<br>The function of this PIN will be updated in future version | 1.8V |

P:POWER    I:INPUT    O:OUTPUT    VDDIO:1.8V

# 5 Dimensions

## 5.1 Module Picture

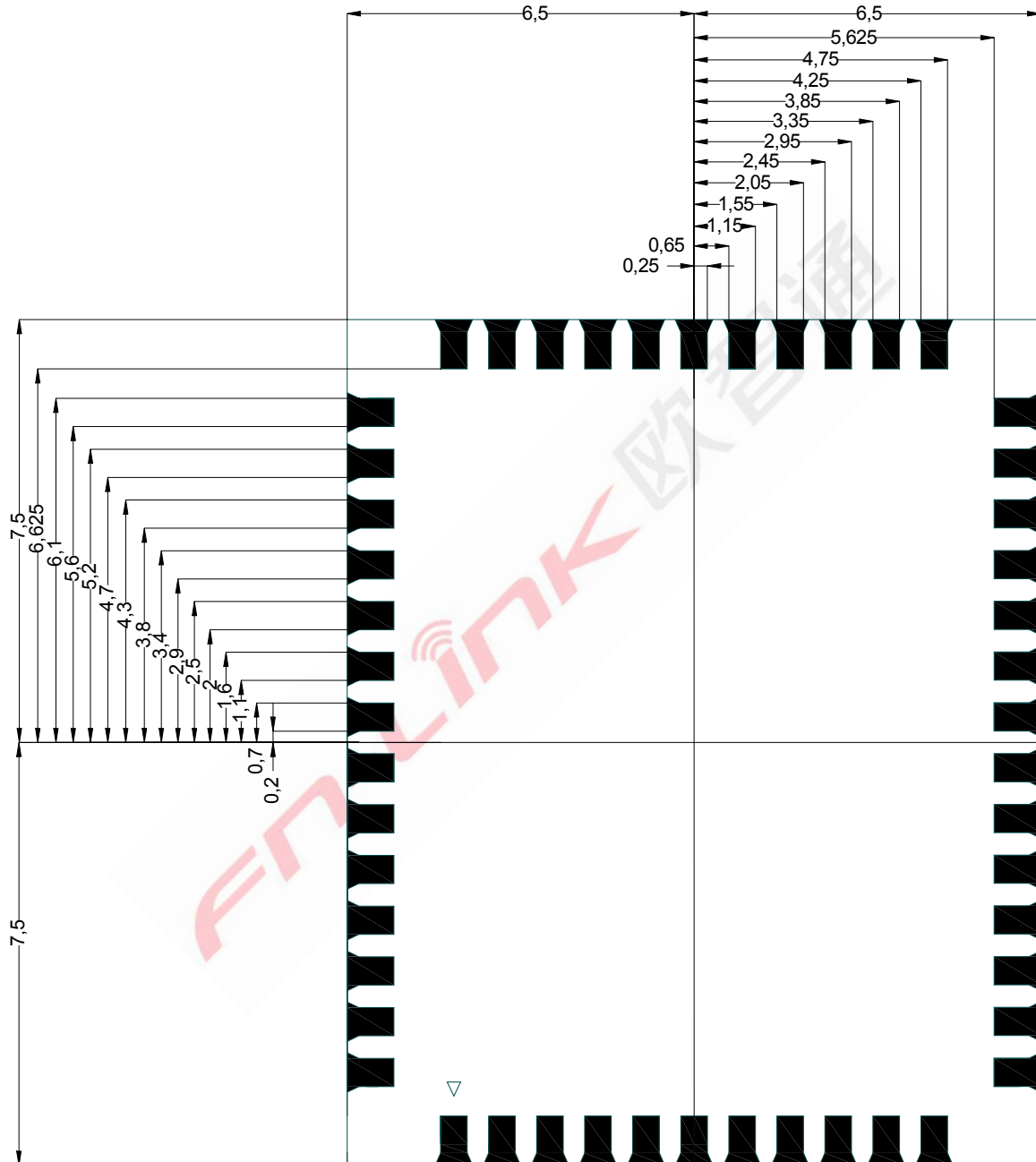| L x W : 15 x 13 (+0.3/-0.1) mm FGK255BSRX-XM:  FGK255BSRX-00:  |  |
|---|---|
| H: 2.15 (±0.2) mm |  |
| **Weight** | 0.81 (±0.1) g |

## 5.2 Marking Description
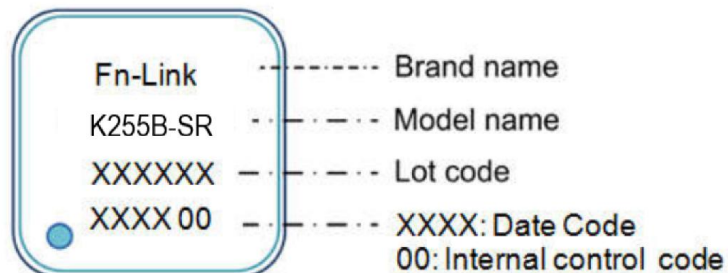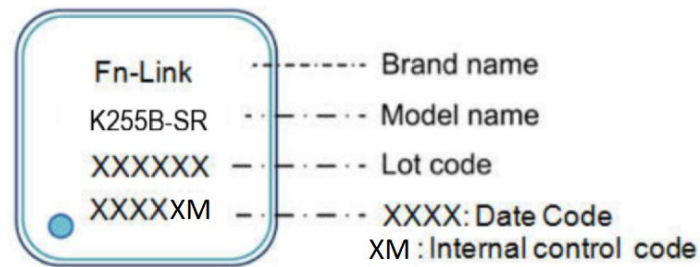
# 5.3 Module Physical Dimensions
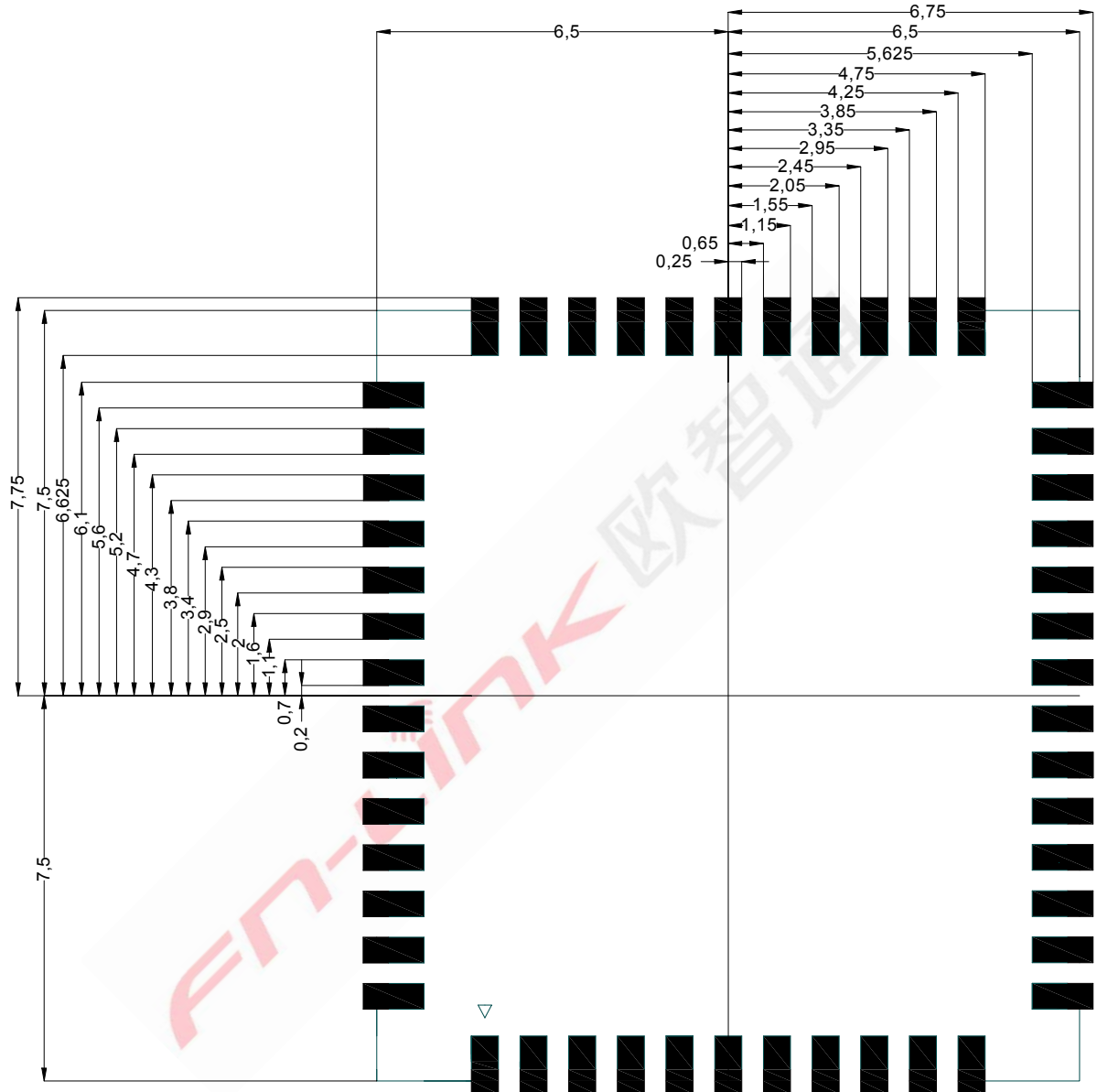
(Unit: mm)

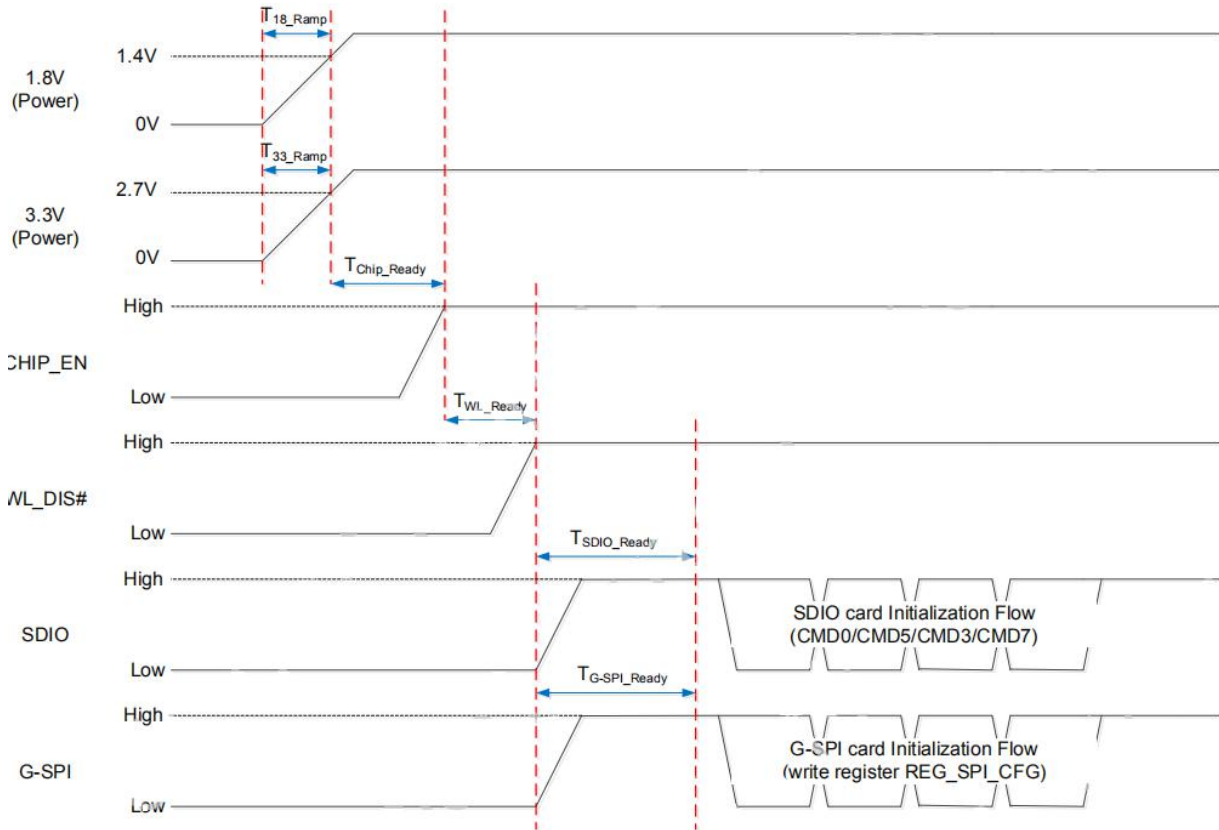< TOP VIEW >

# 5.4 Layout Recommendation

(Unit: mm)

< TOP VIEW >

# 6 Host Interface Timing Diagram

## 6.1 system power on sequence



**System Power-On Sequence**

| | Min | Typical | Max | Unit | Description |
|---|---|---|---|---|---|
| $T_{18\_Ramp}$ | 0.1 | 0.5 | 2.5 | ms | The 1.8V main power ramp up duration. |
| $T_{33\_Ramp}$ | 0.1 | 0.5 | 2.5 | ms | The 3.3V main power ramp up duration. |
| $T_{Chip\_Ready}$ | | | | | CHIP_EN pull high timing |
| $T_{WL\_Ready}$ | | | | ms | WL_DIS# pull high timing |
| $T_{SDIO\_Ready}$ | 1 | 2 | 10 | ms | SDIO Not Ready Duration. In this state, the RTL8821CS may respond to commands without the ready bit being set. After the ready bit is set, the host will initiate complete card detection procedure. |
| $T_{G\text{-}SPI\_Ready}$ | 3 | 4 | 18 | ms | The duration G-SPI device internal initialization. After |

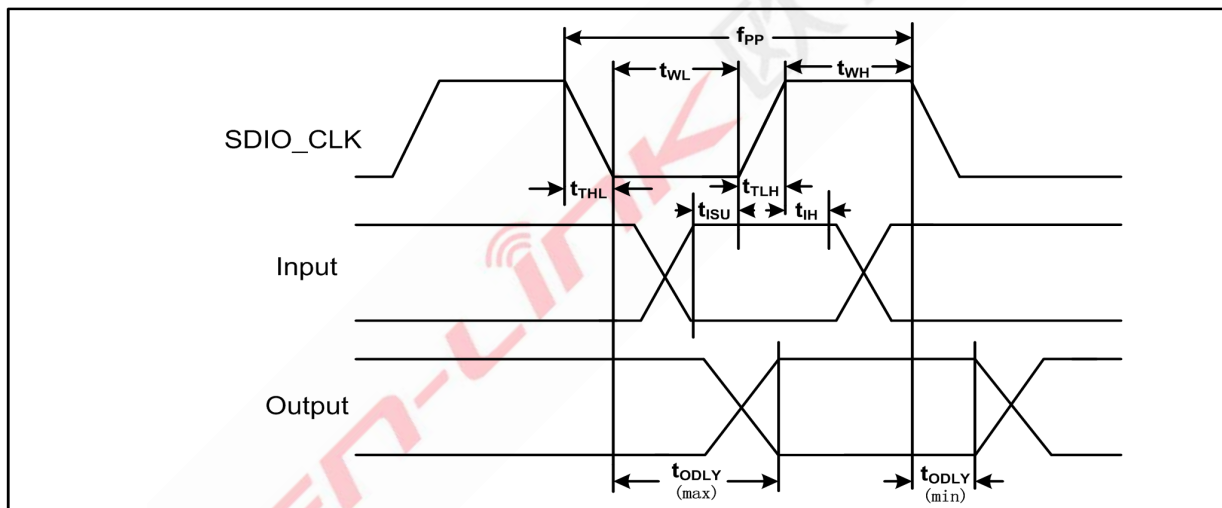## 6.2 SDIO Pin Description

The module supports SDIO version 3.0 for all 1.8V to 3.3V.

**SDIO Pin Description**

| SD 4-Bit Mode | |
|---|---|
| DATA0 | Data Line 0 |
| DATA1 | Data Line 1 or Interrupt |
| DATA2 | Data Line 2 or Read Wait |
| DATA3 | Data Line 3 |
| CLK | Clock |
| CMD | Command Line |

## 6.3 SDIO Default Mode Timing Diagram



| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **SDIO CLK(All values are referred to minimum VIH and maximum VIL[b])** | | | | | |
| Frequency - Data Transfer mode | fPP | 0 | - | 25 | MHz |
| Frequency - Identification mode | fOD | 0 | - | 400 | kHz |
| Clock low time | tWL | 10 | - | - | ns |
| Clock high time | tWH | 10 | - | - | ns |
| Clock rise time | tTLH | - | - | 10 | ns |
| Clock low time | tTHL | - | - | 10 | ns |
| **Inputs:CMD, DAT(referenced to CLK)** | | | | | |
| Input setup time | tISU | 5 | - | - | ns |
| Input hold time | tIH | 5 | - | - | ns |

*Outputs:CMD, DAT(referenced to CLK)*

| | | | | | |
|---|---|---|---|---|---|
| Output delay time - Data Transfer mode | tODLY | 0 | - | 14 | ns |
| Output delay time - Identification mode | tODLY | 0 | - | 50 | ns |

a.   Timing is based on CL ≤ 40 pF load on CMD and Data.

b.   Min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

## 6.4 SDIO High Speed Mode Timing Diagram
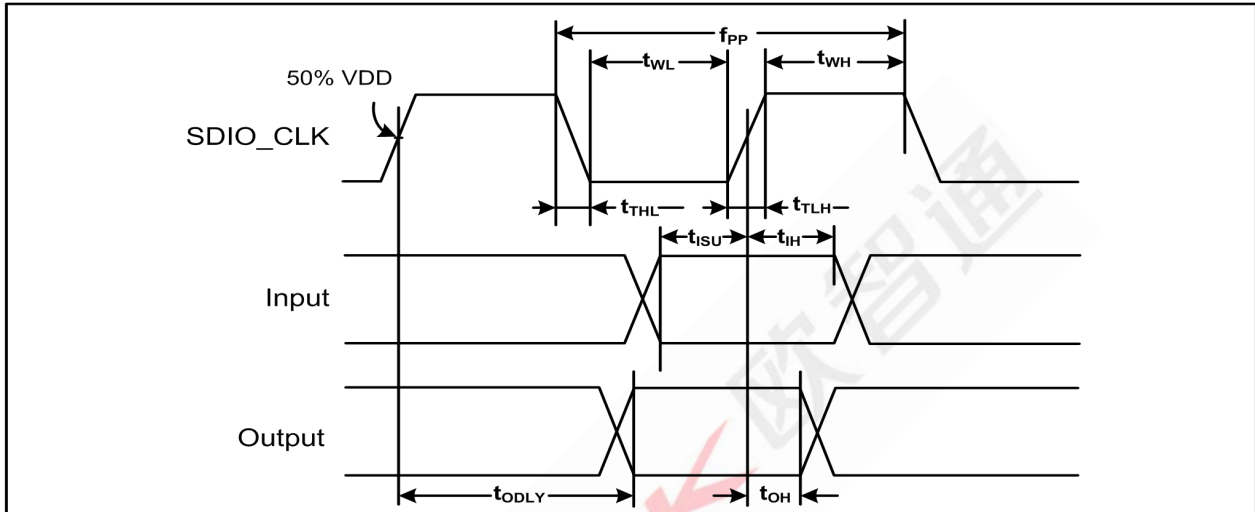


| Parameter | Symbol | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| **SDIO CLK(all values are referred to minimum VIH and maximum VIL[b])** | | | | | |
| Frequency - Data Transfer mode | fPP | 0 | - | 50 | MHz |
| Frequency - Identification mode | fOD | 0 | - | 400 | kHz |
| Clock low time | tWL | 7 | - | - | ns |
| Clock high time | tWH | 7 | - | - | ns |
| Clock rise time | tTLH | - | - | 3 | ns |
| Clock low time | tTHL | - | - | 3 | ns |
| **Inputs:CMD, DAT(referenced to CLK)** | | | | | |
| Input setup time | tISU | 6 | - | - | ns |
| Input hold time | tIH | 2 | - | - | ns |
| **Outputs:CMD, DAT(referenced to CLK)** | | | | | |
| Output delay time - Data Transfer mode | tODLY | - | - | 14 | ns |
| Output delay time - Identification mode | tODLY | 2.5 | - | - | ns |
| Total system capacitance(each line) | CL | - | - | 40 | pF |

a.   Timing is based on CL ≤ 40 pF load on CMD and Data.
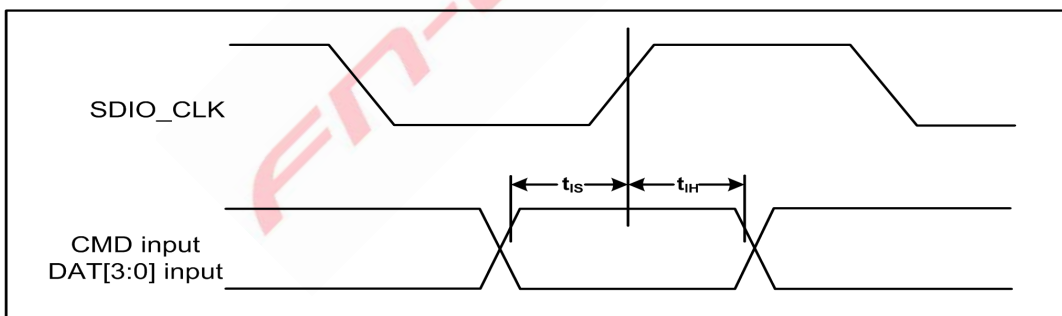
b.   Min(Vih) = 0.7 × VDDIO and max(Vil) = 0.2 × VDDIO.

# 6.5 SDIO Bus Timing Specifications in SDR Modes

Clock timing(SDR Modes)
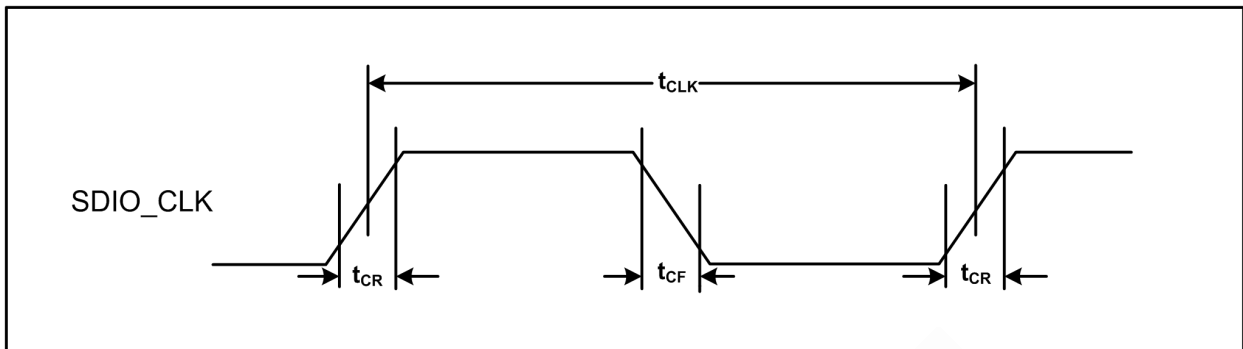


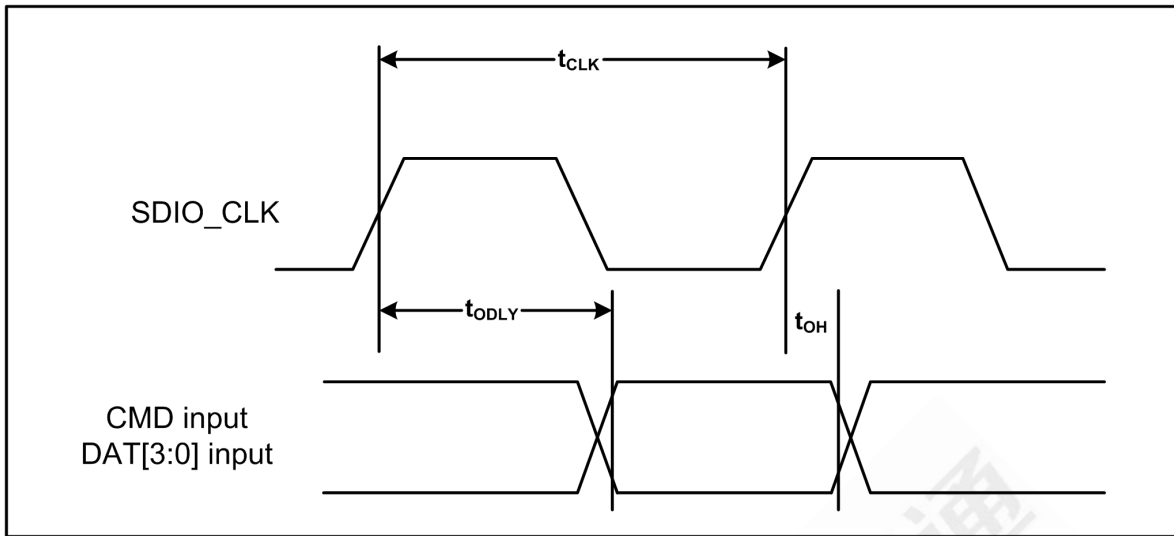| Parametwer | Symbol | Minimum | Maximum | Unit | Comments |
|---|---|---|---|---|---|
| - | $t_{CLK}$ | 40 | - | ns | SDR12 mode |
| | | 20 | - | ns | SDR25 mode |
| | | 10 | - | ns | SDR50 mode |
| | | 4.8 | - | ns | SDR104 mode |
| - | $t_{CR}$, $t_{CF}$ | - | $0.2 \times t_{CLK}$ | ns | $t_{CR}$, $t_{CF}$ < 2.00 ns (max)@100 MHz, $C_{CARD}$ = 10 pF  $t_{CR}$, $t_{CF}$ < 0.96 ns (max)@208 MHz, $C_{CARD}$ = 10 pF |
| Clock duty | - | 30 | 70 | % | - |

Card Input timing (SDR Modes)



| Symbol | Minimum | Maximum | Unit | Comments |
|---|---|---|---|---|
| **SDR104 Mode** | | | | |
| $t_{IS}$ | 1.70[a] | - | ns | $C_{CARD}$ = 10pF, VCT = 0.975V |
| $t_{IH}$ | 0.80 | - | ns | $C_{CARD}$ = 5pF, VCT = 0.975V |
| **SDR50 Mode** | | | | |
| $t_{IS}$ | 3.00 | - | ns | $C_{CARD}$ = 10pF, VCT = 0.975V |
| $t_{IH}$ | 0.80 | - | ns | $C_{CARD}$ = 5pF, VCT = 0.975V |

a. SDIO 3.0 specification value is 1.40 ns.

Card output timing (SDR Modes up to 100MHz)



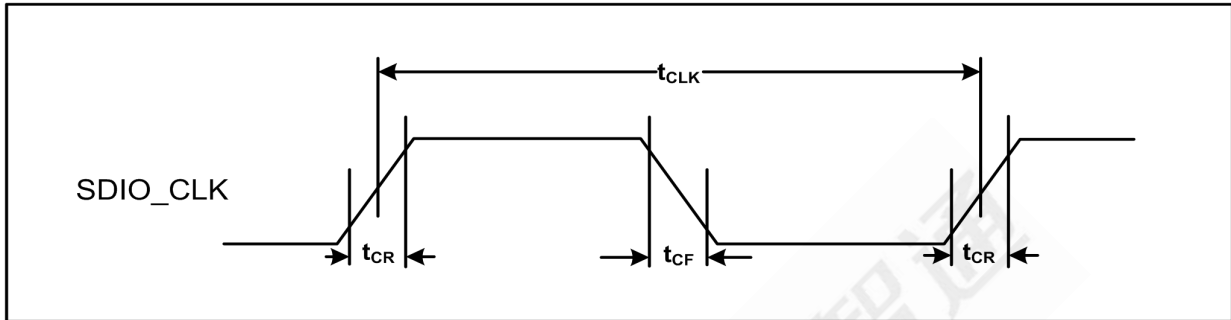| Symbol | Minimum | Maximum | Unit | Comments |
|--------|---------|---------|------|----------|
| $t_{ODLY}$ | - | 7.85[a] | ns | $t_{CLK}\geq$10 ns $C_L$=30 pF using driver type B for SDR50 |
| $t_{ODLY}$ | - | 14.0 | ns | $t_{CLK}\geq$20 ns $C_L$=40 pF using for SDR12, SDR25 |
| $t_{OH}$ | 1.5 | - | ns | Hold time at the $t_{ODLY}$(min) CL=15 pF |

a.   SDIO 3.0 specification value is 7.5 ns.

Card output timing (SDR Modes 100MHz to 208MHz)
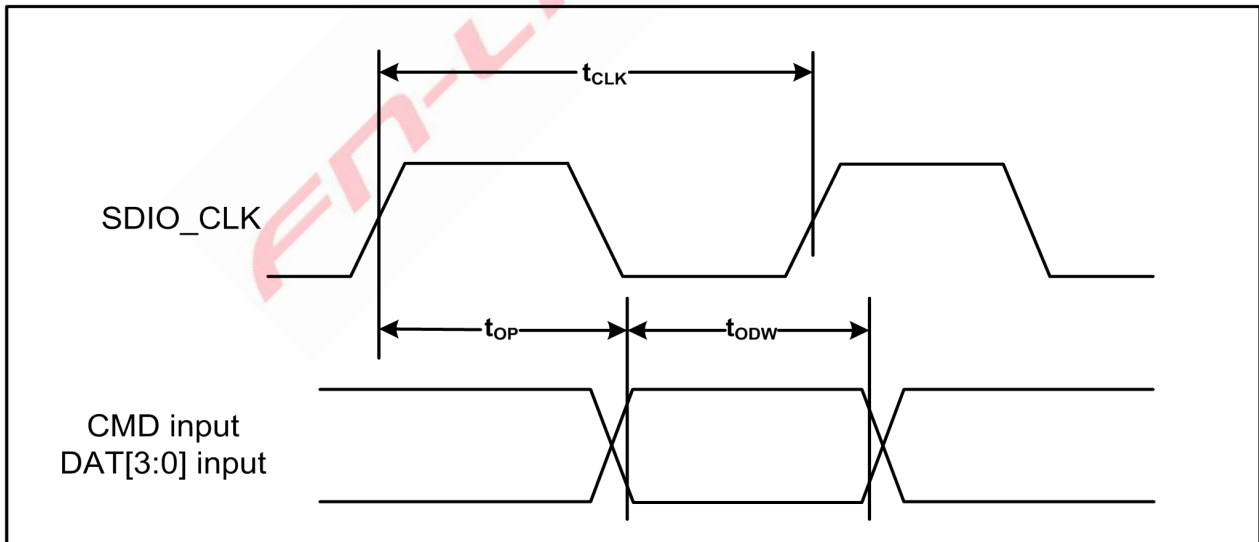


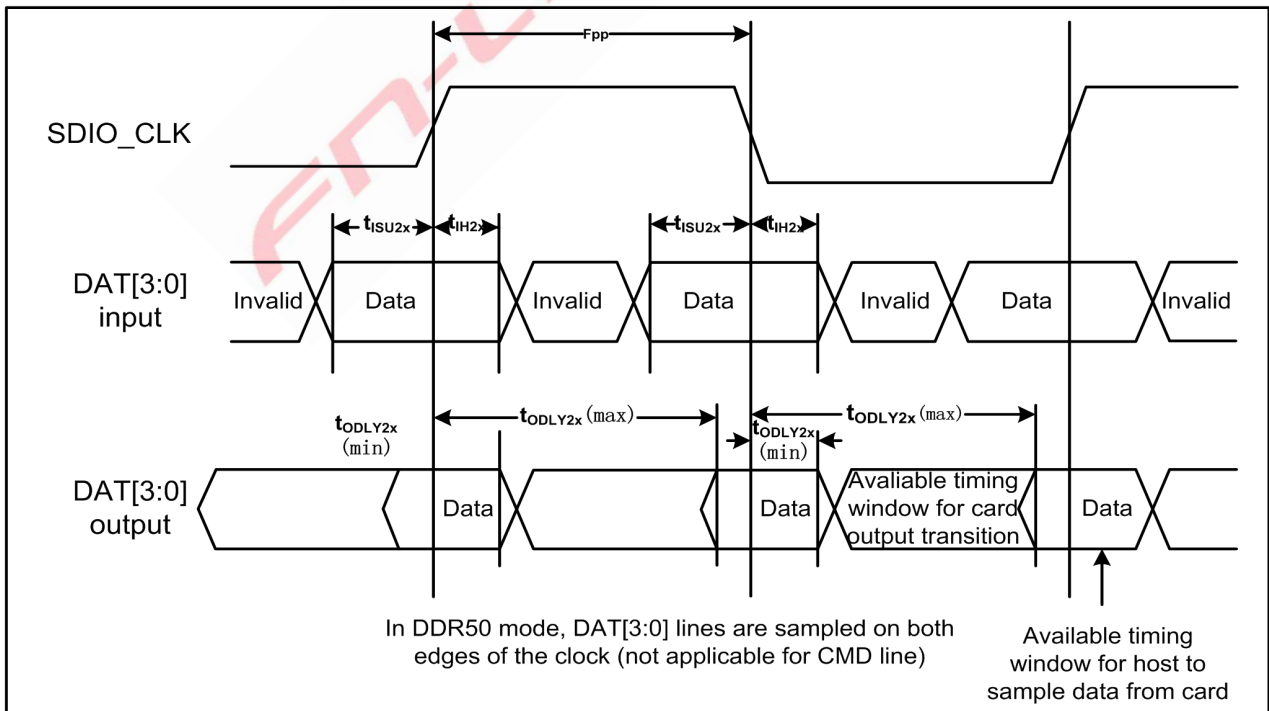| Symbol | Minimum | Maximum | Unit | Comments |
|--------|---------|---------|------|----------|
| $t_{OP}$ | 0 | 2 | UI | Card output phase |
| $\triangle t_{OP}$ | -350 | +1550 | ps | Delay variation due to temp change after tuning |
| $t_{ODW}$ | 0.6 | - | UI | $t_{ODW}$ = 2.88 ns @ 208 MHz |

- $\triangle t_{OP}$ = +1550 ps for junction temperature of $\triangle t_{OP}$ = 90 degrees during operation
- $\triangle t_{OP}$ = -350 ps for junction temperature of $\triangle t_{OP}$ = -20 degrees during operation
- $\triangle t_{OP}$ = +2600 ps for junction temperature of $\triangle t_{OP}$ = -20 to +125 degrees during operation

## 6.6 SDIO Bus Timing Specifications in DDR50 Mode



| parameter | Symbol | Minimum | Maximum | Unit | Comments |
|---|---|---|---|---|---|
| - | $t_{CLK}$ | 20 | - | ns | DDR50 mode |
| - | $t_{CR}$, $t_C$ | - | $0.2 \times t_{CLK}$ | ns | $t_{CR}$, $t_{CF}$ < 4.00 ns (max)@50 MHz, $C_{CARD}$ = 10 pF |
| Clock duty | - | 45 | 55 | % | - |

Data Timing

| parameter | Symbol | Minimum | Maximum | Unit | Comments |
|---|---|---|---|---|---|
| *Input CMD* | | | | | |
| Input setup time | $t_{ISU}$ | 6 | - | ns | $C_{CARD}$ < 10 pF (1 Card) |
| Input hold time | $t_{IH}$ | 0.8 | - | ns | $C_{CARD}$ < 10 pF (1 Card) |
| *Output CMD* | | | | | |
| Output delay time | $t_{ODLY}$ | - | 13.7 | ns | $C_{CARD}$ < 30 pF (1 Card) |
| Output hold time | $t_{OH}$ | 1.5 | - | ns | $C_{CARD}$ < 15 pF (1 Card) |
| *Input DAT* | | | | | |
| Input setup time | $t_{ISU2x}$ | 3 | - | ns | $C_{CARD}$ < 10 pF (1 Card) |
| Input hold time | $t_{IH2x}$ | 0.8 | - | ns | $C_{CARD}$ < 10 pF (1 Card) |
| *Output CMD* | | | | | |
| Output delay time | $t_{ODLY2x}$ | - | 7.85[a] | ns | $C_{CARD}$ < 25 pF (1 Card) |
| Output hold time | $t_{ODLY2x}$ | 1.5 | - | ns | $C_{CARD}$ < 15 pF (1 Card) |

a. SDIO 3.0 specification value is 7.0 ns

# 7 Reference Design
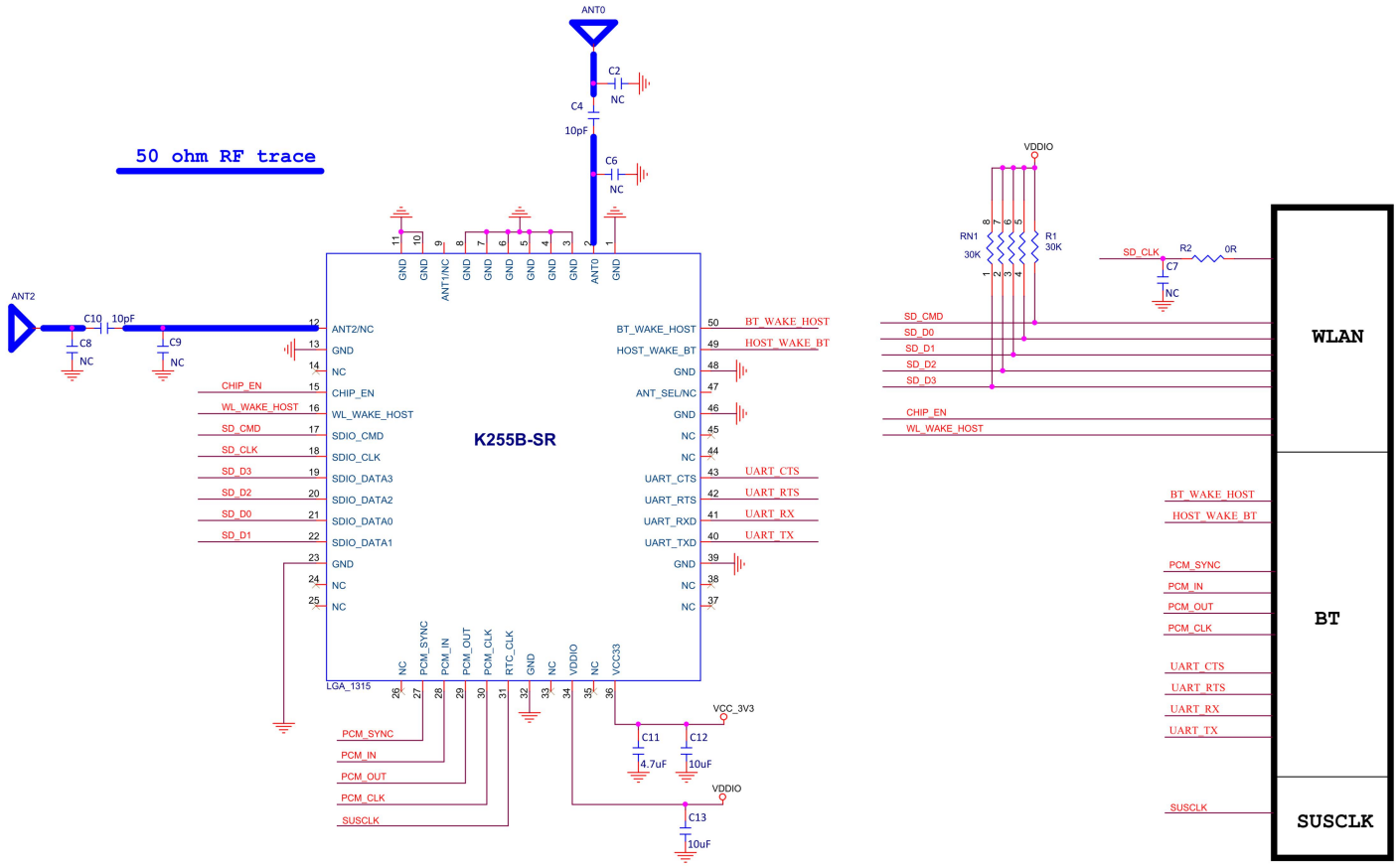


C11, C12 should be placed close to pin 36 of the module
C13 should be placed close to pin 34 of the module

Note: The function of PIN49 and PIN50 will be updated in future version.

# 8 Ordering Information

| Part No. | Description |
|---|---|
| FGK255BSRX-XM | W155S1, a/b/g/n/ac, Wi-Fi, BT5.0, 1T1R, SDIO+UART, 2 Antenna version, 13x15mm(XIAOMI VERSION) |
| FGK255BSRX-00 | W155S1, a/b/g/n/ac, Wi-Fi, BT5.0, 1T1R, SDIO+UART, 2 Antenna version, 13x15mm(GENERAL VERSION) |

# 9 The Key Material List

| Item | Part Name | Description | Manufacturer |
|---|---|---|---|
| 1 | Inductor | 2016  2.2uH,±20% | Sunlord, Ceaiya, Cenker |
| 2 | Diplexer | 1608 Dual-band, dual-mode 2.4GHz/5GHz WLAN | Glead, Walsin, ACX, Murata, MAG.LAYERS |
| 3 | Crystal | 2016 40MHz | ECEC, TKD, Hosonic, JWT, TXC |
| 4 | Chipset | W155S1 | Amlogic |
| 5 | PCB | FR4, 4 LAYER, GREEN | XY-PCB, GDKX, Sunlord, SLPCB |

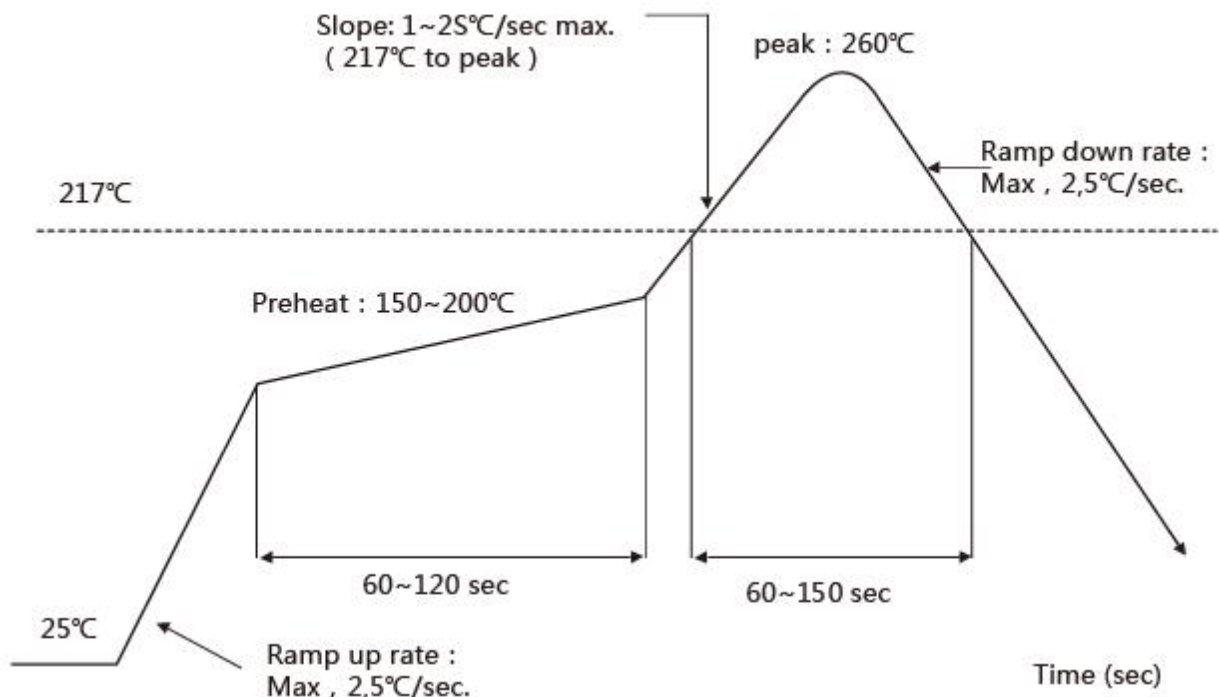# 10 Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : ⩽260°C

Time within 5° C of peak temperature：≥10s

Number of Times : ⩽2 times

# 11 Package Information

## 11.1 Reel

A roll of 1500pcs
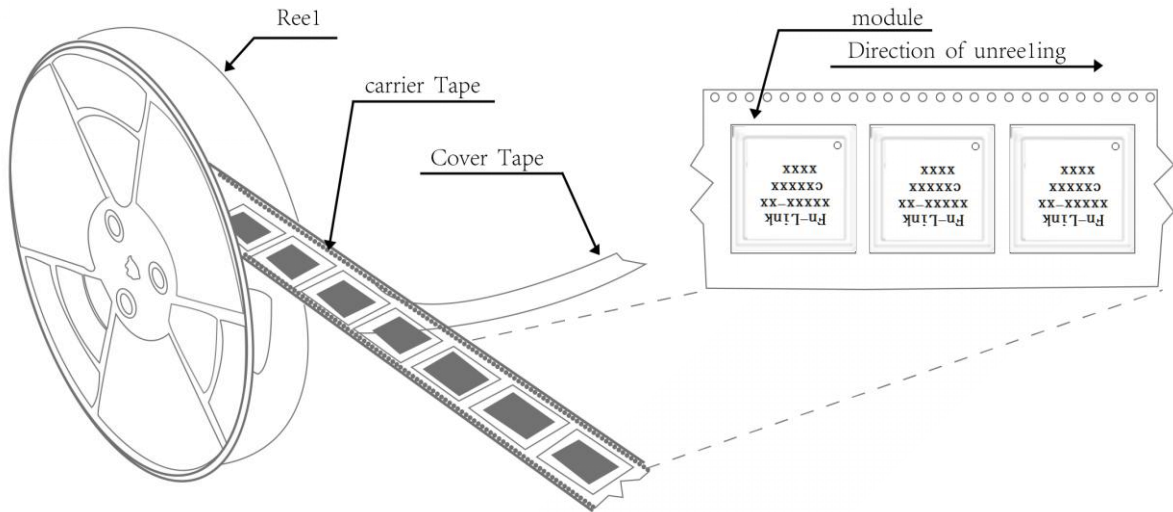


## 11.2 Carrier Tape Detail

| ITEM | W | AO | BO | D | F | E | KO | PO | P2 | P | T |
|------|-----|-------|-------|------------|------------|-------|-------|-------|-------|------|--------|
| DIM | 24 | 13.40 | 15.40 | 1.50 | 11.5 | 1.75 | 2.65 | 4.0 | 2.0 | 16.0 | 0.30 |
| TOLE | +0.3 −0.3 | ±0.15 | ±0.15 | +0.1 −0.0 | +0.1 −0.1 | ±0.1 | ±0.10 | ±0.1 | ±0.1 | ±0.1 | ±0.05 |
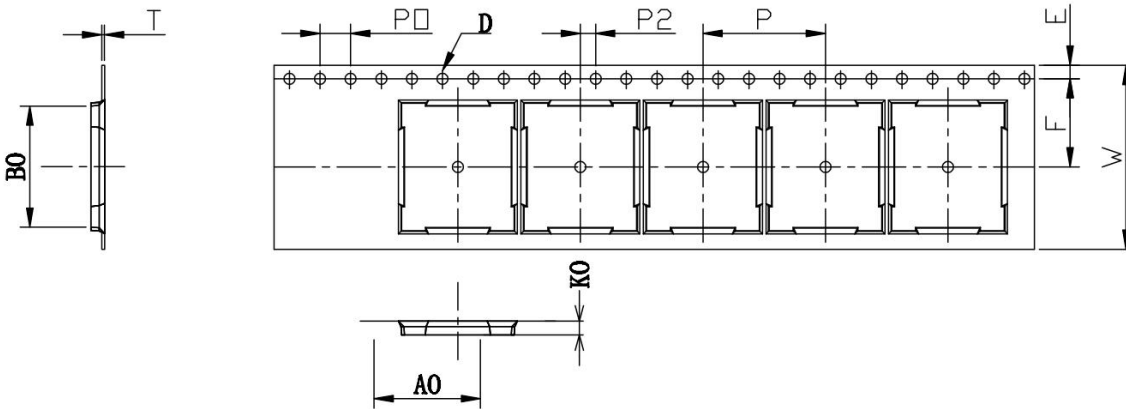
## 11.3 Packaging Detail
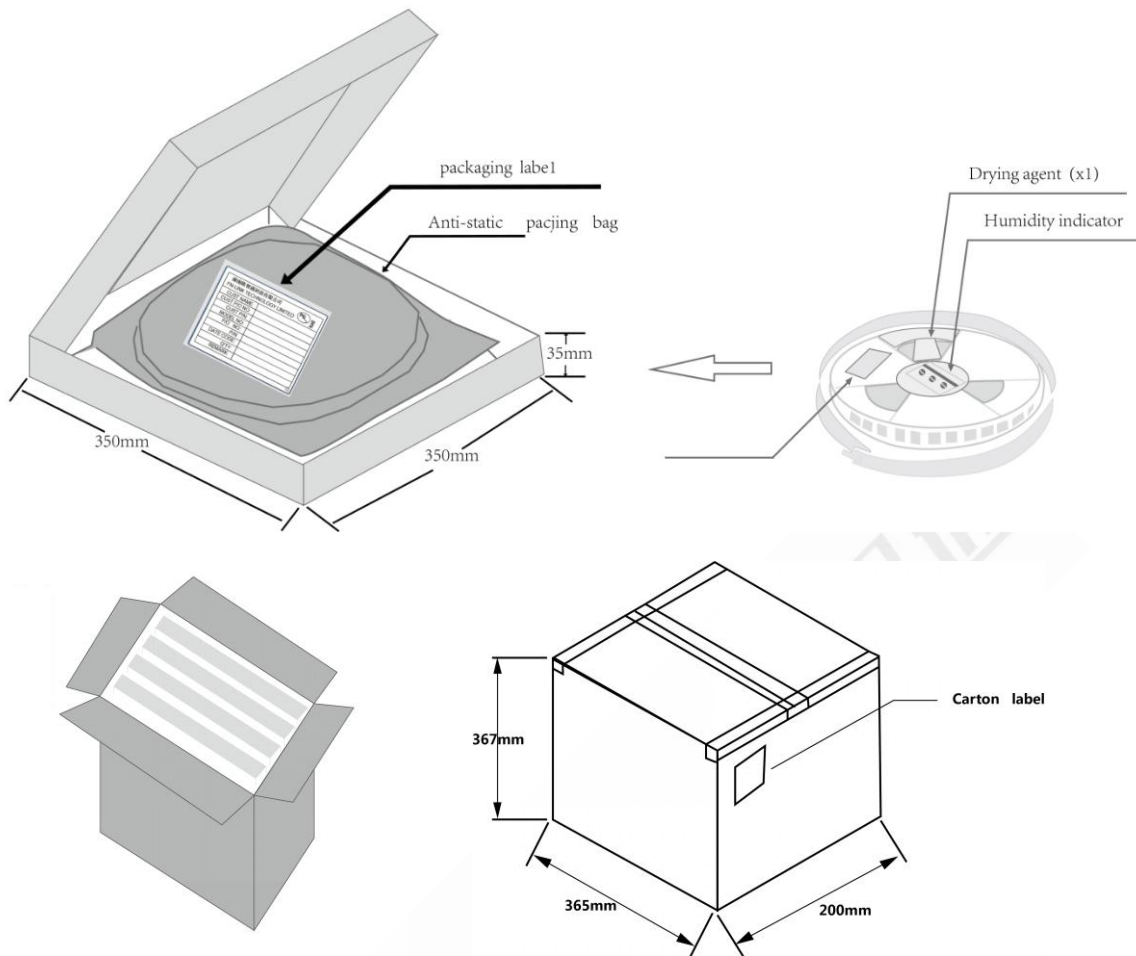


## 11.4 Moisture sensitivity

The Modules is a Moisture Sensitive Device level 3, in according with standard IPC/JEDEC J-STD-020, take care

all the relatives requirements for using this kind of components.

Moreover, the customer has to take care of the following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% relative humidity (RH).

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5.

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) "IPC/JEDEC J-STD-033A paragraph 5.2" is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag indicates 10% RH or more