6223N-SRD

Wi-Fi Single-band 1X1 + Bluetooth 4.2
Combo Module Datasheet

FN-LINK™
Innovation For Surfing

6223N-SRD Module Datasheet

Office: 6 Floor, Building U6, Junxiang U8 Park,
Hangcheng Avenue, Bao'an District,
Shenzhen City, CHINA
Factory: No.8, Litong Road, Liuyang Economic & Technical
Development Zone, Changsha, Hunan, CHINA
TEL: +86-755-2955-8186
Website: www.fn-link.com

Customer Approval : _____ Company

_____ Title

_____ Signature

_____ Date

_____ Fn-Link

Revision History

Version	Date	Revision Content	Draft	Approved
1.0	2020/11/9	New version	fc	

CONTENTS

1 Overview

1.1 Introduction

6223N-SRD is a highly integrated and excellent performance Wireless LAN (WLAN) and BT. It provides SDIO interface for Wi-Fi to connect with host processor and high speed UART interface for BT. High-speed wireless connection up to 150 Mbps and Bluetooth can support BT2.1+EDR/BT3.0 and BT4.2. It can be easily manufactured on SMT process.

This WLAN Module design is based on Realtek RTL8723DS-CG QFN48 4.4X4.4mm(Realtek).It combines a MAC, a 1T1R capable baseband, and RF in a single chip. It is designed to provide excellent performance with low power Consumption and enhance the advantages of robust system and cost-effective.
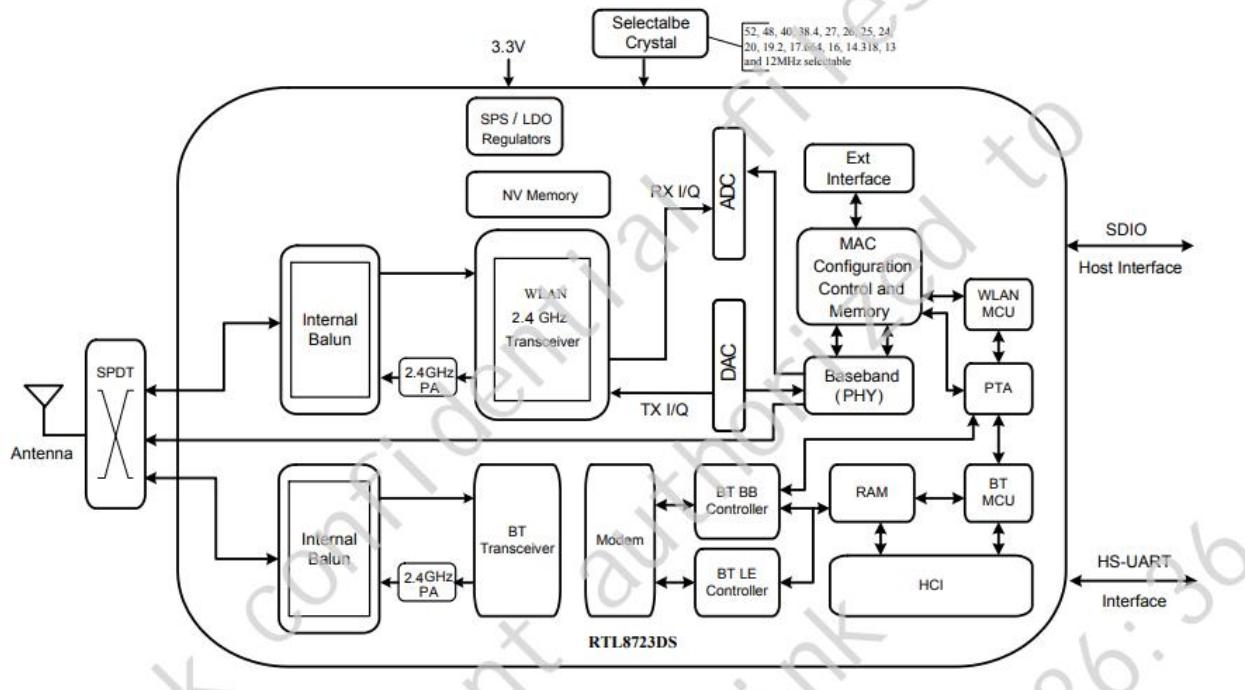
6223N-SRD integrates whole Wi-Fi/BT function blocks into a chip, such as SDIO/UART, MAC, BB, AFE, RFE, PA, EEPROM and LDO/SWR, except fewer passive components remained on PCB.

This compact module is a total solution for a combination of Wi-Fi + BT technologies. The module is specifically developed for Smart phones and Portable devices.

1.2 Features

- Operate at ISM frequency bands (2.4GHz)
- CMOS MAC, Baseband PHY, and RF in a single chip for 802.11b/g/n compatible WLAN
- Wi-Fi 1 transmitter and 1 receiver allow data rates supporting up to 150 Mbps downstream and 150 Mbps upstream PHY rates
- SDIO for Wi-Fi and UART for Bluetooth
- Fully Qualified for Bluetooth 2.1+EDR specification including both 2Mbps and 3Mbps modulation mode
- Fully qualified for Bluetooth 3.0
- Fully qualified for Bluetooth 4.2 Dual mode
- Full_speed Bluetooth operation with Piconet and Scatternet support

Block Diagram:

1.3 General Specification

Model Name	6223N-SRD
Product Description	Support Wi-Fi/BT functionalities
Dimension	L x W x T: 23 x 21 x 4.8 (typical) mm
BT Interface	Support UART
Wi-Fi Interface	Support SDIO 2.0
Operating temperature	0°C to 70°C
Storage temperature	-40°~125°

1.4 Recommended Operating Rating

	Min.	Typ.	Max.	Unit
Operating Temperature	0	25	70	deg.C
VBAT	3.0	3.3	3.6	V
VDDIO	1.7	1.8 or 3.3	3.6	V

2 General Specification

2.1 Wi-Fi RF Specifications
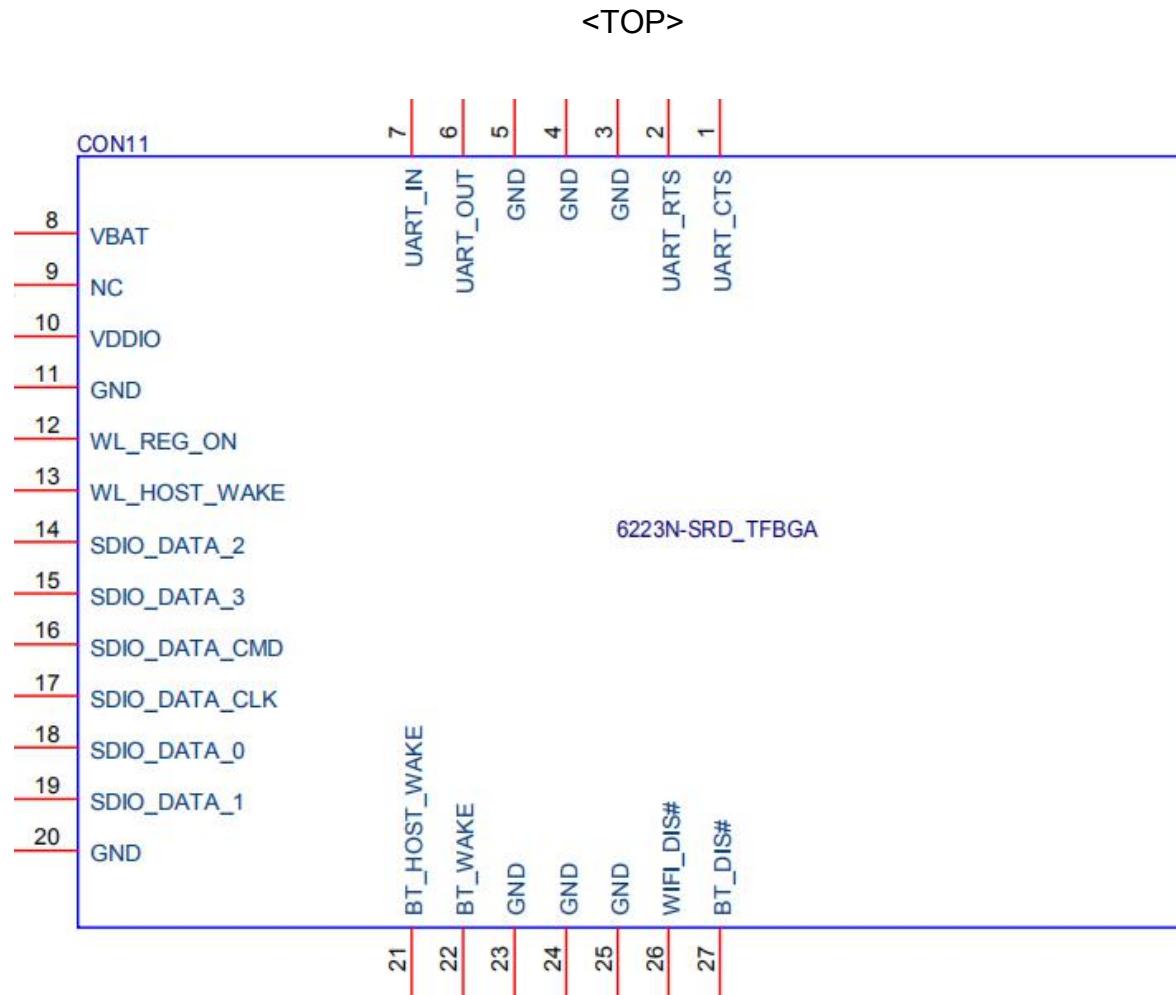
| Feature	Description
WLAN Standard	IEEE 802.11b/g/n, Wi-Fi compliant
Frequency Range	2.4GHz~2.497GHz
Channels	2.4GHz:CH1~CH13
Output Power	802.11b /11Mbps:17dBm $\pm$ 1.5dB@EVM<=-10dB
	802.11g /54Mbps:14dBm $\pm$ 1.5dB@EVM<=-25dB
	802.11n/MCS7@HT20:13dBm $\pm$ 1.5dB@EVM<=-28dB
	802.11n/MCS7@HT40:13dBm $\pm$ 1.5dB@EVM<=-28dB
Spectrum Mask	IEEE compliant
Freq. Tolerance	$\pm$15 ppm
Receive Sensitivity (11b) @8% PER	802.11b/11Mbps: PER@≤-76
Receive Sensitivity (11g) @10% PER	802.11g/54Mbps: PER@≤-65
Receive Sensitivity (11n,20MHz) @10% PER	802.11n/MCS7@HT20: PER@≤-64
Receive Sensitivity (11n,40MHz) @10% PER	802.11n/MCS7@HT40: PER@≤-61

2.2 Bluetooth Specification

Feature	Description		
General Specification			
Bluetooth Standard	Bluetooth V4.2 of 1, 2 and 3 Mbps.		
Host Interface	UART		
Frequency Band	2402 MHz ~ 2480 MHz		
Number of Channels	79 channels		
Modulation	GFSK, π/4-DQPSK and 8DPSK		
RF Specification			
	Min.	**Typical.**	**Max.**
Output Power (Class 1.5)		6dBm	
Output Power (Class 2)		2dBm	
Sensitivity @ BER=0.1% for GFSK (1Mbps)		-86dBm	
Sensitivity @ BER=0.01% for π/4-DQPSK (2Mbps)		-86dBm	
Sensitivity @ BER=0.01% for 8DPSK (3Mbps)		-80dBm	
Maximum Input Level	GFSK (1Mbps): -20dBm		
	π/4-DQPSK (2Mbps) : -20dBm		
	8DPSK (3Mbps) : -20dBm		
Sensitive @PER=30.8% FOR BLE		-90dBm	

3 Pin Assignments

3.1 Pin Outline

<TOP>

6223N-SRD_TFBGA

3.2 Pin Definition
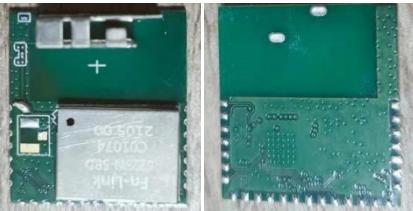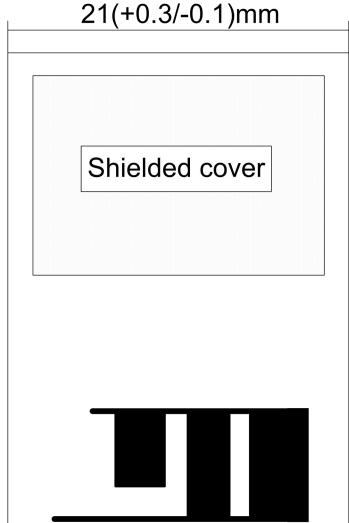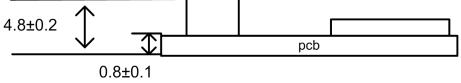
NO.	Name	Type	Description	Voltage
1	UART-CTS		UART-CTS	VDDIO
2	UART-RTS		UART-RTS	VDDIO
3	GND		Ground connections	
4	GND		Ground connections	
5	GND		Ground connections	
6	UART-OUT	O	UART output	VDDIO
7	UART-IN	I	UART input	VDDIO
8	VBAT	P	Supply 3.3V	3.3V
9	NC		Floating (Don't connected to	

| 10	VDDIO	P	I/O Voltage supply input 1.8V to 3.3V	1.8V ~ 3.3V
11	GND		Ground connections	
12	CHIP_EN	I	chip enable pin, default pull high	3.3V
13	WL_WAKE_HOST	I/O	WLAN device wake-up host	1.8V ~ 3.3V
14	SD_D2	I/O	SDIO Data line 2	1.8V ~ 3.3V
15	SD_D3	I/O	SDIO Data line 3	1.8V ~ 3.3V
16	SD_CMD	I/O	SDIO Command Input	1.8V ~ 3.3V
17	SD_CLK	I	SDIO Clock Input	1.8V ~ 3.3V
18	SD_D0	I/O	SDIO Data line 0	1.8V ~ 3.3V
19	SD_D1	I/O	SDIO Data line 1	1.8V ~ 3.3V
20	GND		Ground connections	
21	BT_HOST_WAKE		BT host wake-up device	VDDIO
22	BT_WAKE_HOST		BT device wake-up host	VDDIO
23	GND		Ground connections	
24	GND		Ground connections	
25	GND		Ground connections	
26	WIFI_DIS#		Pull high: ON , Pull low: OFF External pull low can disable WL	
27	BT_DIS#		Pull high: ON , Pull low: OFF External pull low can disable BT	
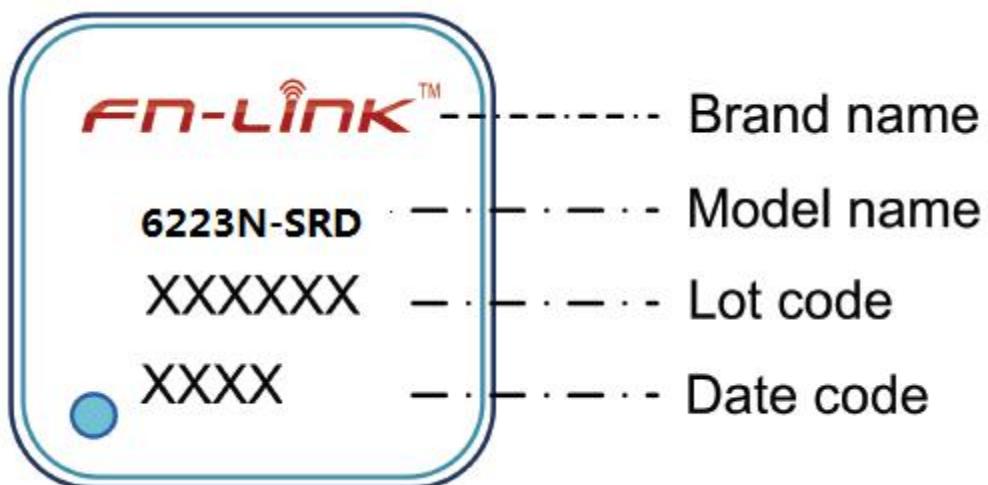
P:POWER   I:INPUT   O:OUTPUT

4 Dimensions

4.1 Module Picture

L x W : 23 x 21 (+0.3/-0.1) mm	21(+0.3/-0.1)mm Shielded cover 23(+0.3/-0.1)mm
H: 4.8 (±0.2) mm	4.8±0.2 pcb 0.8±0.1
Weight	1.65g

4.2 Marking Description

FN-LINK™ ------- Brand name

6223N-SRD —·—·—· Model name

XXXXXX —··—··— Lot code

XXXX —·—·—·· Date code
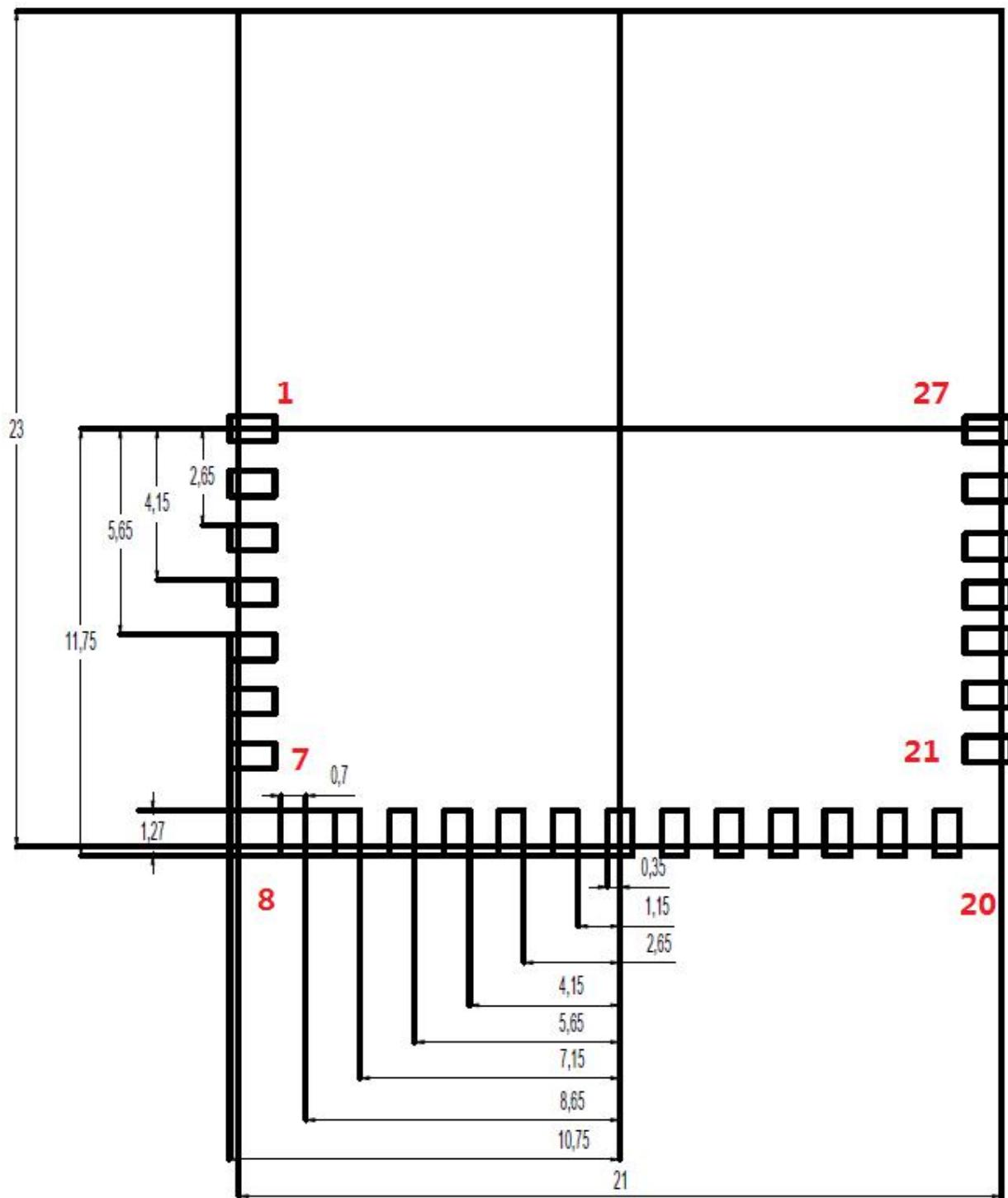
# 4.3 Module Physical Dimensions
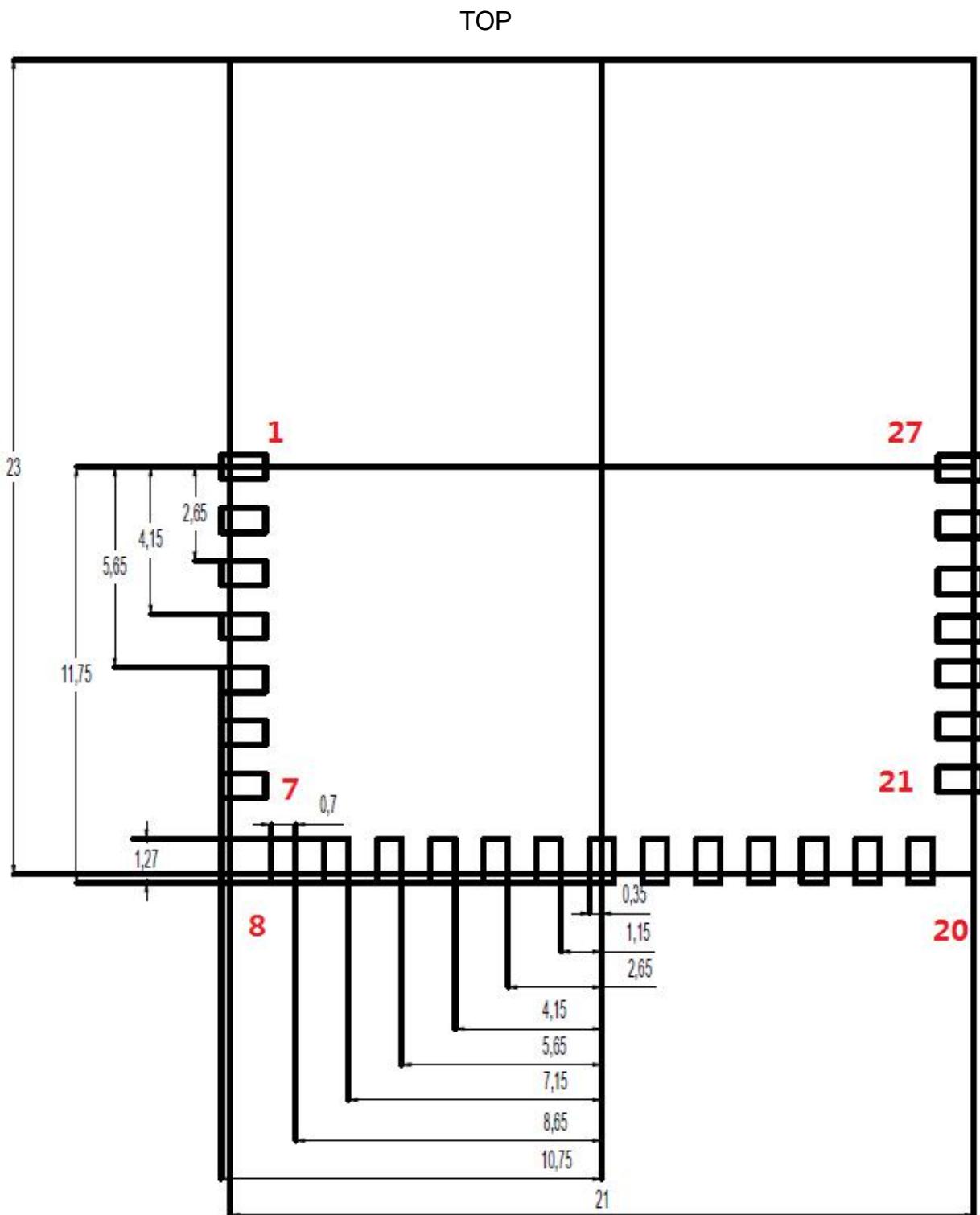
(unit: mm)

(TOP)

4.4 Layout Reference

(unit: mm)

TOP

6 Host Interface Timing Diagram
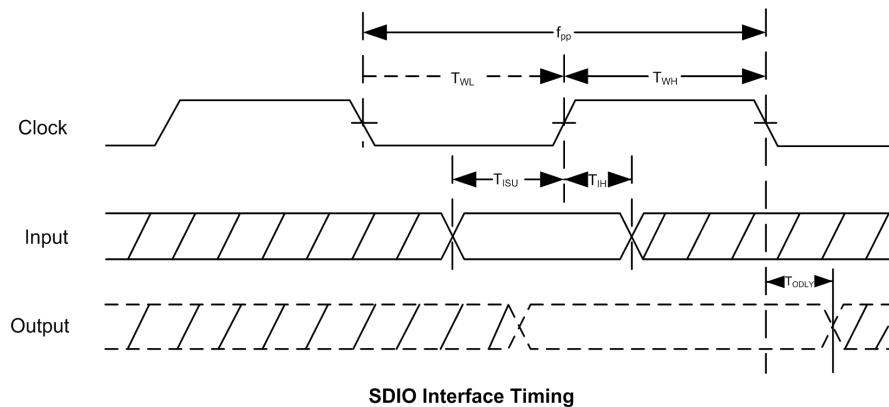
6.1 SDIO Pin Description

The module supports SDIO version 2.0 for all 1.8V 4-bit UHSI speeds: SDR12(25 Mbps), and SDR25(50Mbps) in addition to the 3.3V default speed(25MHz) and high speed (50 MHz). It has the ability to stop the SDIO clock and map the interrupt signal into a GPIO pin. This 'out-of-band' interrupt signal notifies the host when the WLAN device wants to turn on the SDIO interface. The ability to force the control of the gated clocks from within the WLAN chip is also provided.

SDIO Pin Description

SD 4-Bit Mode	
DATA0	Data Line 0
DATA1	Data Line 1 or Interrupt
DATA2	Data Line 2 or Read Wait
DATA3	Data Line 3
CLK	Clock
CMD	Command Line
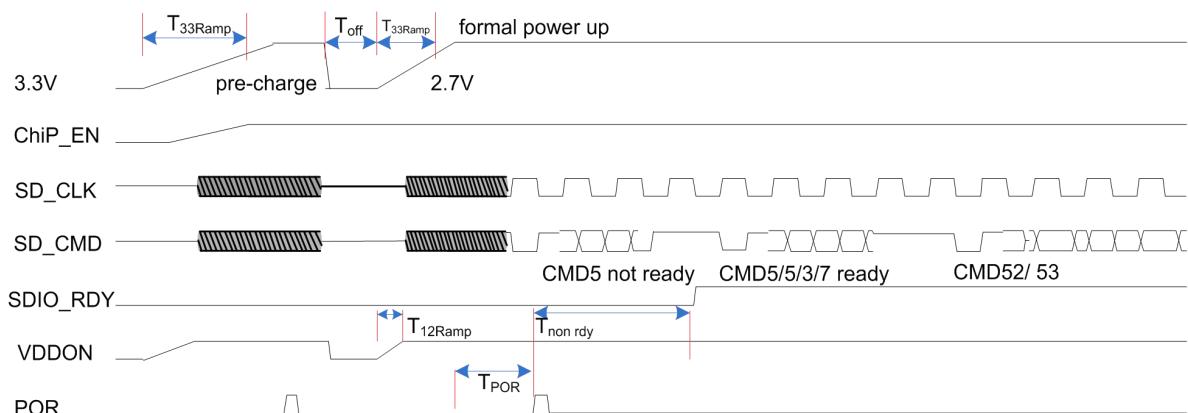
6.2 SDIO Default Mode Timing Diagram

SDIO Interface Timing

SDIO Interface Timing Parameters

NO	Parameter	Mode	MIN	MAX	Unit
f_{pp}	Clock Frequency	Default	0	25	MHz
		HS	0	50	MHz
T_{WL}	Clock Low Time	DEF	10	-	ns
		HS	7	-	ns
T_{WH}	Clock High Time	DEF	10	-	ns
		HS	7	-	ns
T_{ISU}	Input Setup Time	DEF	5	-	ns
		HS	6	-	ns
T_{IH}	Input Hold Time	DEF	5	-	ns
		HS	2	-	ns
T_{ODLY}	Output Delay Time	DEF	-	14	ns
		HS	-	14	ns

6.3 SDIO Power-on sequence

Symbol	Min	Typical	Max	Unit
T_{33ramp}	0.2	-	No Limit	ms
T_{off}	250	500	1000	ms
T_{33ramp}	0.2	0.5	2.5	ms
T_{12ramp}	0.1	0.5	1.5	ms
T_{POR}	2	2	8	ms
T_{non_rdy}	1	2	10	ms

6.4 UART Interface Characteristics

The RTL8723DS UART interface is a standard 4-wire interface with RX,TX,CTS and RTS. The interface supports the Bluetooth 2.0 UART HCI H4 and H5 specifications. The default baud rate is 115.2K baud. In order to support high and low speed baud rate,the RTL8723DS provides multiple UART clocks.
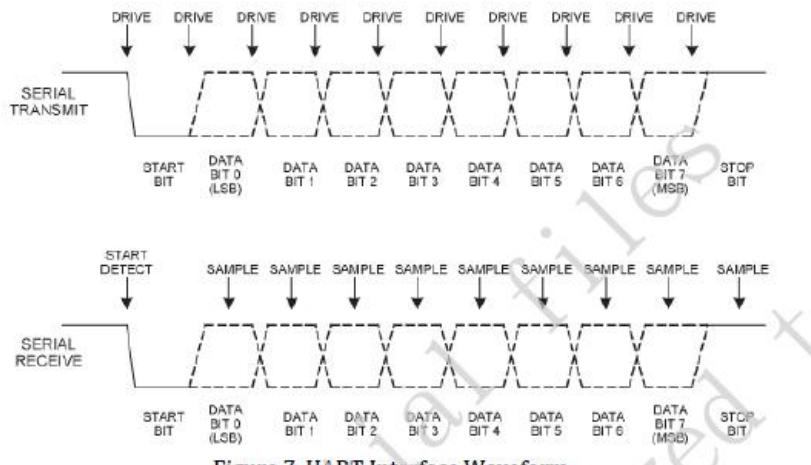

Figure 7. UART Interface Waveform

# 6.5 UART Interface Power-on Sequence
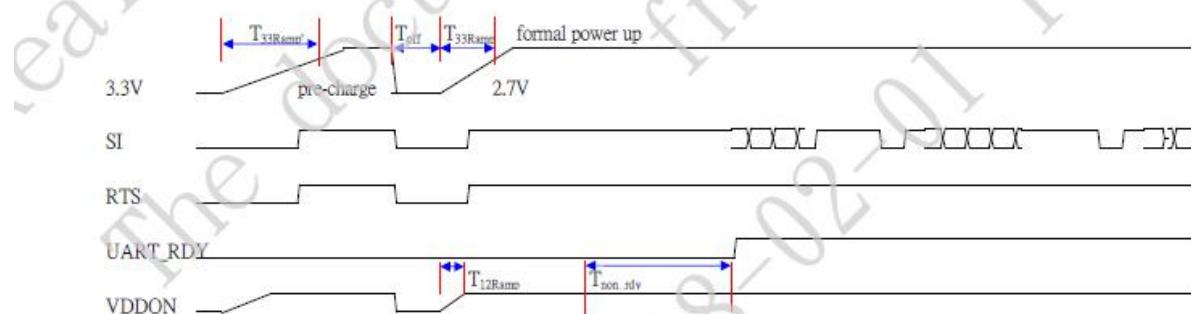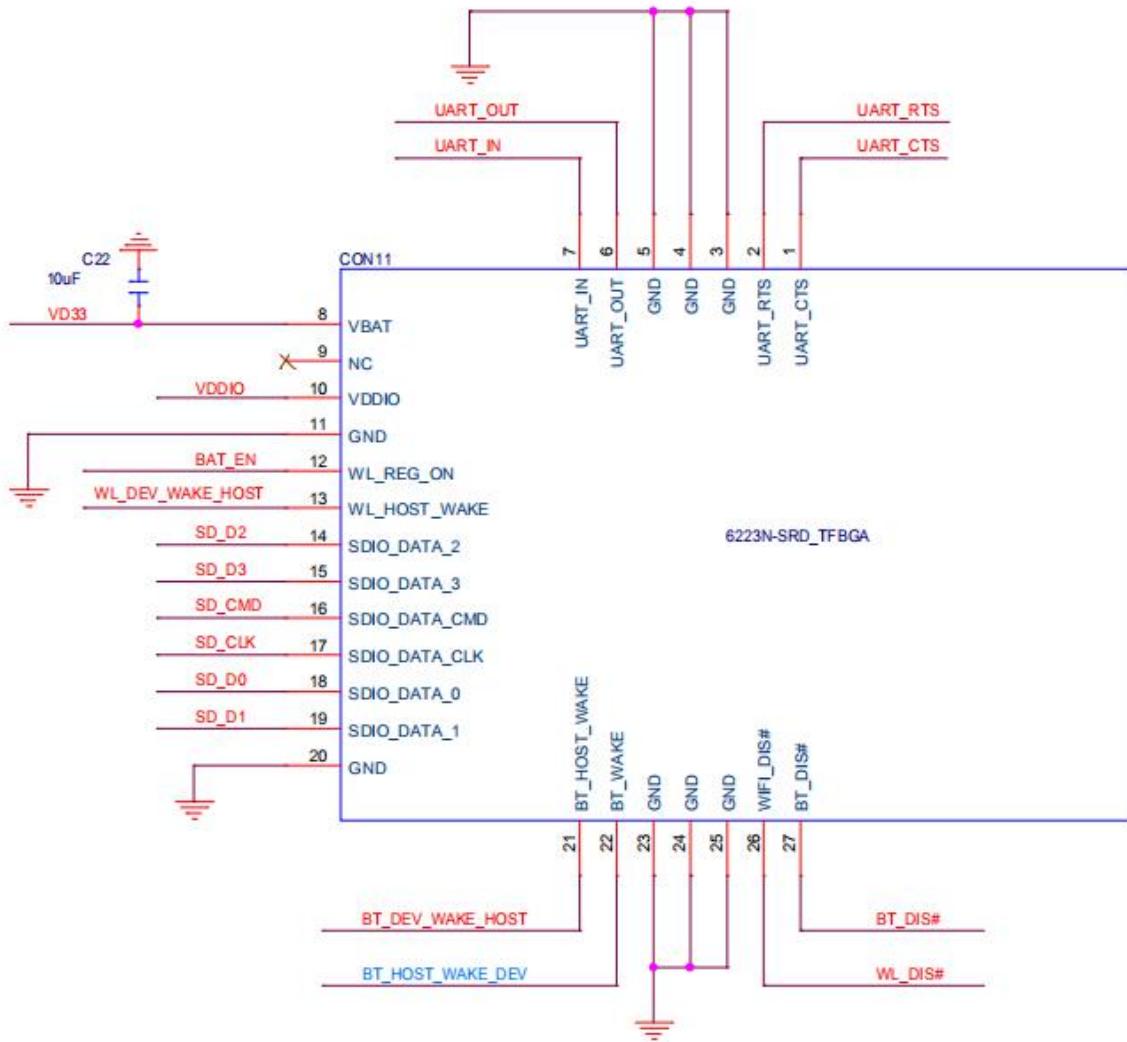
Figure 8. UART Power-On Sequence With Hardware Flow Control

7 Reference Design

Note:

1. BAT_EN could not use for module power off, please switch the 3.3V power for module on/off.

2.please keep the antenna on no metal area.

8 Ordering Information

Part No.	Description
FG6223NSRD-00	RTL8723DS,b/g/n,wifi1T1R,21*23.21mm,SDIO+UART,with metal antenna.

9 The Key Material List
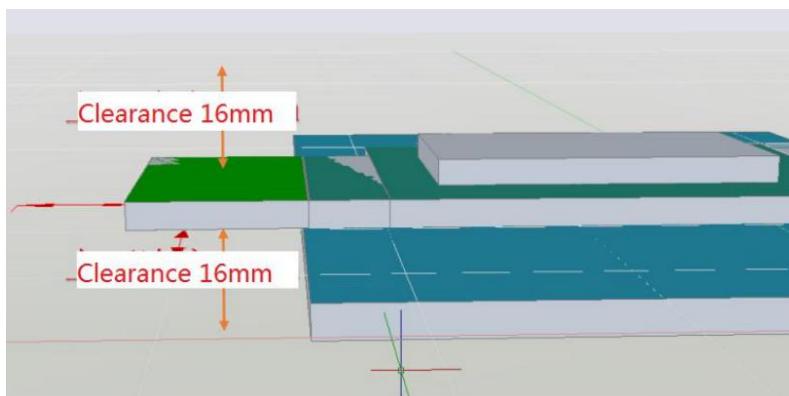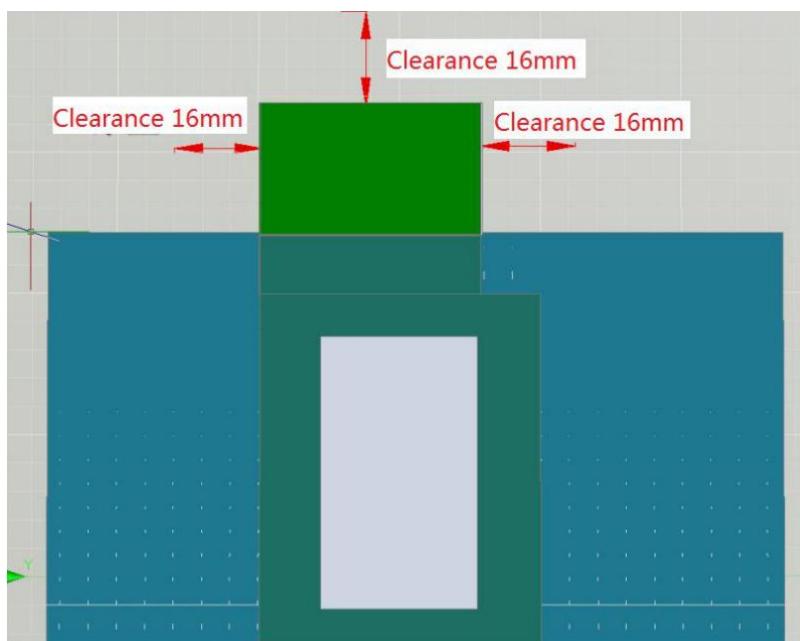
Main	Shielding cover	6223NSRD V1.0 Shielding cover no insulation layer 14.8X11mm-full height of 1.4 copper, no positioning pin(信太)
Alternative	Shielding cover	6223NSRD V1.0 Shielding cover no insulation layer 14.8X11mm-full height of 1.4 copper, no positioning pin (精力通)
Main	Crystal	3225 24MHZ CL=12pF, ±10ppm (东晶)
Alternative	Crystal	3225 24MHZ CL=12pF, ±10ppm (泰晶)
Alternative	Crystal	3225 24MHZ CL=12pF, ±10ppm (晶威特)
Alternative	Crystal	3225 24MHz CL=12pF ±10ppm (鸿星)
Alternative	Crystal	3225 24MHz CL=12pF ±10ppm (TXC)
Main	TVS	0201 5V 0.05pF 15KV TVS (Murata)
Alternative	TVS	0201 5V 0.05pF 15KV TVS (Sunlord)
Alternative	TVS	0201 5V 0.05pF 15KV TVS (维安)
Main	Main Chipset	RTL8723DS-CG QFN48 4.4X4.4mm (Realtek)
Main	antenna	6223N-SRD metal antenna.
Main	PCB	6223N-SRD-V1.0,FR4,green,21X23X0.8mm (翔宇)
Alternative	PCB	6223N-SRD-V1.0,FR4,green,21X23X0.8mm（广东科翔）
Alternative	PCB	6223N-SRD-V1.0,FR4,green,21X23X0.8mm（顺络）
Alternative	PCB	6223N-SRD-V1.0,FR4,green,21X23X0.8mm（深联）

10 Fatness

Fatness of module 6223N-SRD ≤ 0.1mm

11 Antenna clearance area requirements

When using PCB antenna on Wi-Fi module, make sure the distance between PCB on motherboard and other metal devices is at least 16mm.The shaded areas in the figure below need to be marked away from metal devices, sensors, interference sources, and other materials that may interfere with the signal.
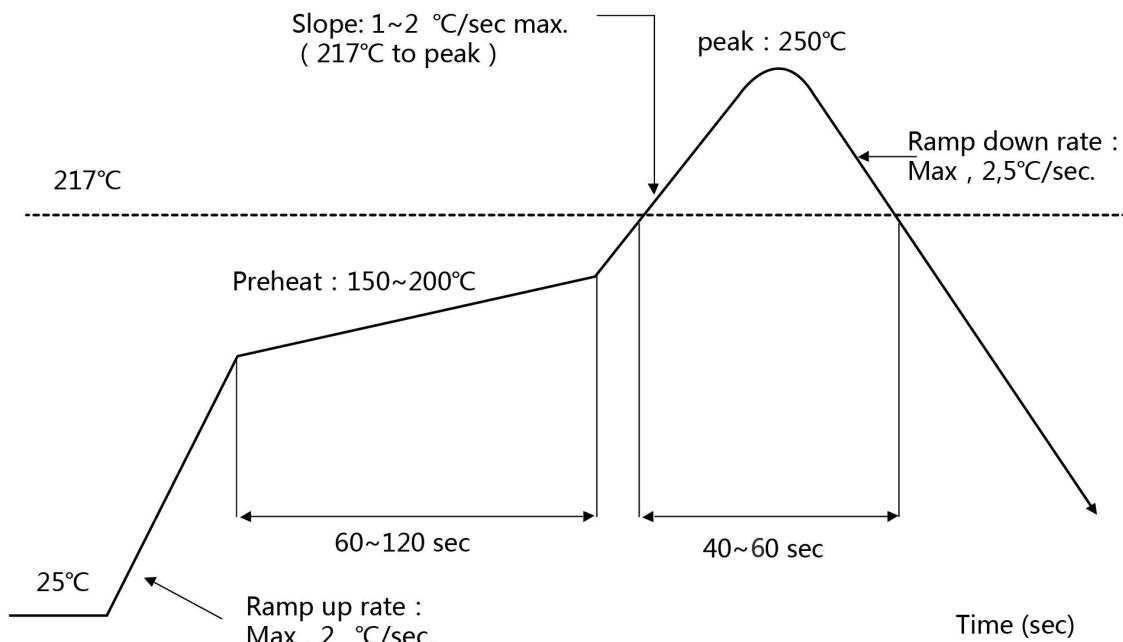
12 Environmental Requirements

12.1 Recommended Reflow Profile

Referred to IPC/JEDEC standard.

Peak Temperature : <250°C

Number of Times : ≤2 times

12.2 Patch Wi-Fi/BT modules installed before the notice

Wi-Fi/BT module installed note:
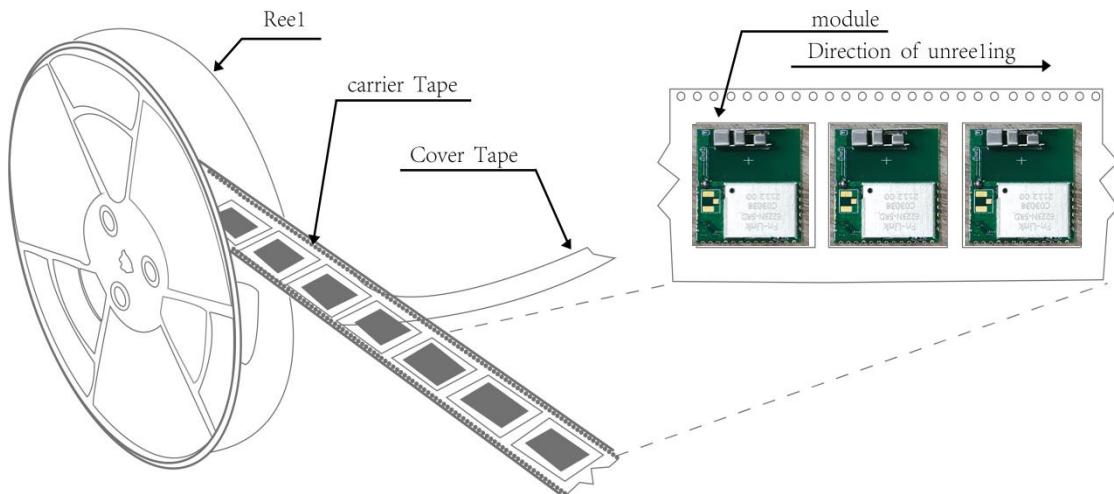
1. Please press 1 : 1 and then expand outward proportion to 0.7 mm, 0.12 mm thickness When open a stencil.

2. Take and use the WIFI/BT module, please insure the electrostatic protective measures.

3. Reflow soldering temperature should be according to the customer the main size of the products, such as the temperature set at 250 + 5 ℃ for the MID motherboard.

About the module packaging, storage and use of matters needing attention are as follows:

1. The module of the reel and storage life of vacuum packing: 1). Shelf life: 8 months, storage environment conditions: temperature in: < 40 ℃, relative humidity: < 90% r.h.

2. The module vacuum packing once opened, time limit of the assembly:

Card:1) check the humidity display value should be less than 30% (in blue), such as: 30% ~ 40% (pink), or greater than 40% (red) the module have been moisture absorption.

2.) factory environmental temperature humidity control: $\leqq$ -30 ℃, $\leqq$ 60% r.h..

3). Once opened, the workshop the preservation of life for 168 hours.

3. Once opened, such as when not used up within 168 hours:

1). The module must be again to remove the module moisture absorption.

2). The baking temperature: 125 ℃, 8 hours.

3). After baking, put the right amount of desiccant to seal packages.

13 Package Information

13.1 Reel

A roll of 2000pcs

13.2 Packaging Details

The take-up package:

Using self-adhesive tape
Color of plastic disc: blue

NY bag size: TBD

Internal box size: TBD

Carton size: TBD

13.3 Moisture Sensitivity

The modules is a Moisture Sensitive Level 3 device, in according with standard IPC/JEDEC J-STD-020, take care of all the requirements for this kind of components. Moreover, please pay attention to following conditions:

a) Calculated shelf life in sealed bag: 12 months at <40°C and <90% RH

b) Environmental condition during the production: 30°C / 60% RH according to IPC/JEDEC J-STD-033A paragraph 5

c) The maximum time between the opening of the sealed bag and the reflow process must be 168 hours if condition

b) IPC/JEDEC J-STD-033A paragraph 5 is respected

d) Baking is required if conditions b) or c) are not respected

e) Baking is required if the humidity indicator inside the bag Indicates 10% RH or more